# AN INVESTIGATION INTO THREE-LEVEL FERROELECTRIC MEMORY

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## Abstract

*Ferroelectric random-access memory (FeRAM) is an emerging nonvolatile memory technology that has several key advantages over flash memory, including much greater program-erase endurance and much faster write speed. However, FeRAM array storage capacities currently lag behind those of flash memory by more than three orders of magnitude; consequently, FeRAM has so far tended to be used only in niche applications, such as smart cards and electronic metering. Significant increases in FeRAM storage density will require progress on many technical fronts. Most digital memory technologies use two possible data signal levels to encode one bit per storage cell. Multilevel cell flash memory uses four data signal levels to increase the storage density to two bits per cell. In this paper we report the results of a preliminary study that investigated the possibility of using three data signal levels to increase the array storage density from 1 bit per cell to an average of 1.5 bits per cell. The principal challenge is to ensure the accurate writing of the three signal states (ferroelectric film polarized in the "up" and "down" directions, and a depolarized film) and the reliable sensing of cell states in the presence of noise and inevitable device parameter variations.*

***Keywords**: ferroelectric memory, multilevel signaling, ternary signaling, ternary memory, multilevel cells.*

## 1. Introduction

Ferroelectric random-access memory (FeRAM) is an emerging technology for nonvolatile memory (NVM) that has several important advantages over mainstream flash memory [1]. For example, flash memory cells can be programmed and erased at most $10^6$ times whereas the endurance of FeRAM cells is now at least $10^{12}$ program-erase cycles [2]. Also, flash memory cells require relatively complex write sequences that can take hundreds of milliseconds to complete whereas FeRAM cells can be written deterministically in under 50 ns. Further advantages are that FeRAM cells can be operated using a low power supply voltage (e.g. ≤ 1.8V) and they can be integrated into a standard CMOS technology using as few as two extra masks [3]. Flash memory requires relatively large program and erase voltages (e.g. ~10 V) that require on-chip charge pumps and high-voltage-tolerant distribution networks. Also, flash memory cells require a second layer of polysilicon, to form the programmable floating gates, and the creation of a uniformly thin tunneling barrier. Recent progress in FeRAM scaling and process integration could pave the way for the successful introduction of embedded FeRAM into high-density Systems-on-a-Chip (SoCs) [3].

Flash memory devices, however, are already available in multi-gigabit device densities whereas the largest FeRAM parts are available only in 1 megabit densities [4]. As the long-time incumbent NVM technology, flash memory benefits from massive levels of research and development investment. Increases in FeRAM storage density will require much further progress on FeRAM cell miniaturization, improvements in reference voltage generation and cell signal sensing circuitry, and better understanding and control of the long-term stability of the properties of the required ferroelectric materials.

In this paper we present the results of a preliminary simulation-based study that investigated the possibility of using three-level (i.e., ternary) signaling to increase the storage density of FeRAM cells [5]. The nonlinear polarization characteristic of ferroelectric materials, such as lead zirconium titanate (PZT), makes it very difficult to implement the four-level signaling that is used in multilevel cell (MLC) flash memory. Instead, we considered the use of three-level signals, where the three cell states are (1) polarization in the "up" direction across the film, (2) polarization in the opposite "down" direction across the film, and (3) no net polarization across the film (i.e., a suitably depolarized film). If each cell can store one of three states, then pairs of cells can store nine distinct joint states. Only eight of those states are required to encode three bits, implying an average storage density of 1.5 bits per cell. (Such an encoding has been used previously in experimental multilevel DRAMs at the University of Alberta [6,7].) The translation to and from external binary information to ordered pairs of ternary values can be readily

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accomplished using combinational logic in the peripheral circuitry.

The rest of this paper is organized as follows: The next section reviews conventional binary FeRAM operation, while section 3 describes the operation of the proposed ternary FeRAM. Section 4 describes how the effects on ternary FeRAM operation of inevitable device parameter variations were modeled in our simulation study. Section 5 summarizes the results of that study. Finally, section 6 makes some concluding remarks.

## 2. Binary FeRAM Operation

FeRAM exploits a defining property of a class of materials, called ferroelectrics, in which a reversible remanent electric polarization can be imposed on the ferroelectric by applying an external electric field. The polarization behaves like regions of immobile charge of opposite sign that appear on opposite surfaces of the dielectric. The behaviour of a ferroelectric is described by a hysteresis loop, like the one shown in Figure 1. A ferroelectric film could start out with a "down" remanent polarization –Pr at point A in the loop. When a positive external field is applied in the "up" direction, the polarizations of the individual microscope domains of the ferroelectric start to re-orient themselves to be more aligned with that field. After traveling up along the lower branch of the loop to point B, a coercive electric field strength +Ec is reached such that, if the field were to be removed, there would be no net remanent polarization in the dielectric; that is, the dielectric would be left depolarized. If, on the other hand, the applied field is increased further in strength to point C, the degree of polarization in the dielectric reaches a saturation value +Ps. Removing the applied field then causes the upper branch of the hysteresis loop to be followed down to point D, which corresponds to an "up" remanent polarization of +Pr. Pulsing the external electric field in the opposite direction causes the loop to be traced from point D through to points E to F and then back to A.

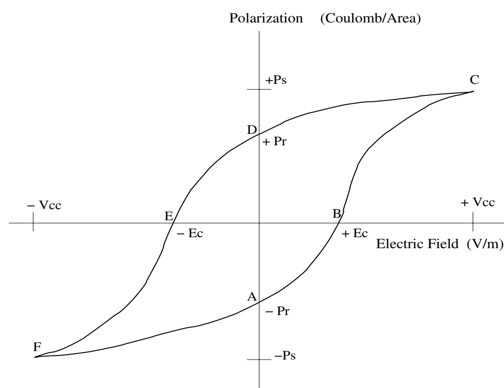


Fig. 1 Ferroelectric Hysteresis Loop Characteristic

Conventional binary FeRAM uses the remanent polarizations corresponding to points A and D on the hysteresis loop to store the two binary values. We will arbitrarily assume that points A and D are used to encode binary values "1" and "0", respectively. (In our proposed ternary FeRAM, the third state will be the depolarized state at the origin of the polarization characteristic. The states corresponding to points A and D would then no longer simply encode "1" and "0", as will be explained later.)

Production FeRAMs use one of two cell designs. The 1T-1C cell design, shown in Figure 2(a), is very similar to a conventional DRAM cell. The major differences are that the storage capacitor dielectric is replaced with a thin film of ferroelectric (e.g. PZT), and that the "lower" terminal of the capacitor is driven by a switched plate line (PL) signal instead of being held at a constant plate potential (e.g. $\frac{1}{2}V_{DD}$). As in a DRAM cell, the state of the cell is sensed by a sense amplifier circuit (not shown) via a bit line (BL) and an access transistor switch controlled by a word line (WL). The sense amplifier is a fast differential-mode comparator circuit that rapidly determines the sign of the potential difference between the cell signal and an appropriately generated reference signal. Figure 2(b) shows the bulkier 2T-2C cell design. The advantage of this cell is that it is self-referencing: the two bitline signals, BL and BLN, that are connected to the cell carry complementary signals that can be compared directly by the sense amplifier, with no need for a separately generated reference signal. The 2T-2C design offers more robust operation, due to the roughly double-strength signal charge, at the cost of a roughly halved storage density.

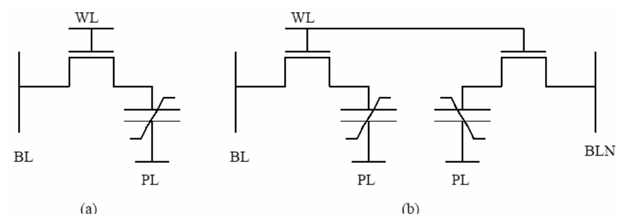


Fig. 2 1T-1C and 2T-2C FeRAM Cell Designs

Figure 3 shows the key waveforms that are involved in a read operation to a 1T-1C FeRAM cell. First, BL is precharged to 0 V by asserting control signal PRE. When PRE is de-asserted, BL is isolated and left floating at 0 V. Address decoder logic receives the row address, decodes it, and asserts high the corresponding WL. This connects the "upper" (storage) node of the cell capacitor to BL. After this event, the PL is pulsed from 0 V up to the positive supply voltage $V_{DD}$. The ferroelectric cell capacitor is sized during design so that the PL signal will cause the polarization of the cell to be switched if the polarization is initially opposed to the applied field. If the initial polarization is aligned with the PL-generated field, then the polarization increases in strength slightly when the field is applied, but retains the same direction. In the case of a polarization reversal, a relatively large positive charge is



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dumped onto BL due mostly to the switched ferroelectric polarization, indicating a stored “1”; otherwise, there is no polarization reversal in the cell ferroelectric and a smaller positive charge appears on the BL indicating a stored “0”. The BL signal is still relatively weak at this point, so it must be amplified by a differential-mode sense amplifier that compares the BL signal with a reference BL signal that is midway in potential between the expected “0” and “1” BL signals. There are various ways of generating the required reference signal [1].

Note that the read operation is destructive because the act of sensing a stored “1” changes the polarization state of the cell to a “0” (for a stored “0” the polarization direction remains unchanged). Read operations to an FeRAM cell must therefore be followed by a write back operation that restores the original data (or substitutes newly written data for a write operation), in the same way as in a DRAM read operation. A write back is accomplished by simply returning the PL back to 0 V with the BL held at the amplified full-swing value. Referring to the points in Figure 1, sensing a “1” followed by writing back a “1” corresponds to tracing through the loop from A to C (pulse the PL, switch the cell polarization, and sense the BL), then to F (write back the “1”), and then back to A (leave a stored “1”). Sensing a “0” involves tracing through the loop from D to C (pulse the PL without switching the cell polarization and sense the BL), then stay at C (write back the “0”), and then back to D (leave a stored “0”).

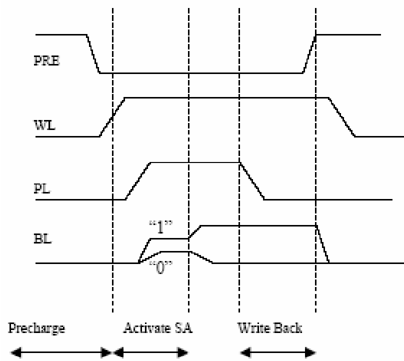


Fig. 3 Destructive Read Operation in Binary FeRAM

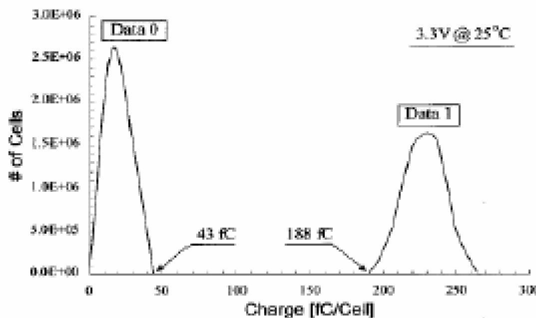


Fig. 4 BL Signal Distributions in a Binary FeRAM [8]

Figure 4 shows the distribution of the expected “0” and “1” signals on the BL [8]. The “1” signal distribution is higher in voltage because of the presence of the switched ferroelectric charge, which is absent in the “0” signal. The areas of the two distributions will be the same (if properly normalized) but the “1” distribution will tend to have a greater variance, and hence a lower peak probability density, than the “0” distribution [3].

## 3. Ternary FeRAM Operation

Multilevel signal operation requires the creation of accurate stored data signals (i.e., polarization states) during write operations, and the creation of accurate reference bitline signals for sensing during read operations. In addition, to maximize the signal-noise-ratio during sensing, it is important to use widely-spaced nominal data signals. A further challenge in a multilevel FeRAM cell is the nonlinearity in the ferroelectric hysteresis characteristic, which makes it difficult to control the remanent dielectric polarization. For these reasons, we chose to reuse the same two nonzero remanent polarizations as conventional binary FeRAM (which will now no longer simply encode “0” and “1”), and to add the depolarized condition as the third cell state. We will denote the three states as “L” (replacing “0”), “M” and “H” (replacing “1”). Figure 5 shows the BL voltage distributions that one would expect to be produced when sensing these three cell states. The middle distribution for M arises from the new depolarized state. Clearly for the ternary encoding to work, there must be a sufficiently large gap (e.g., about 100 mV) between the L and H distributions. Indeed, there must be a sufficiently large noise margin between the L and M distributions, and the M and H distributions; otherwise, sensing errors will occur.

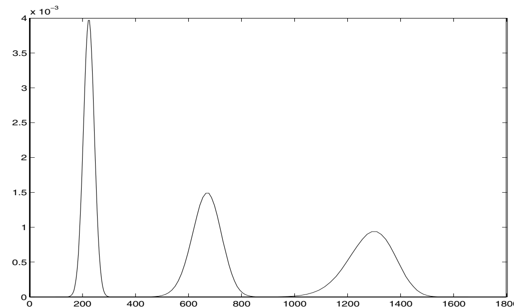

Fig. 5 BL Voltage Distributions in a Ternary FeRAM

As described earlier, the signal levels in pairs of cells are interpreted together to produce an average storage capacity of 3 bits per cell pair (i.e., 1.5 bits per cell). One of many possible encodings is shown in the table below.

| | |
|---|---|
| “LL” ⇔ “000” | “MM” ⇔ “100” |
| “LM” ⇔ “001” | “MH” ⇔ “101” |
| “LH” ⇔ “010” | “HL” ⇔ “110” |
| “ML” ⇔ “011” | “HM” ⇔ “111” |


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The proposed ternary FeRAM poses numerous technical challenges [5]. The L and H signals can be written in the same way as 0 and 1 signals, respectively, in a conventional binary FeRAM, but the M signal requires a fast way of depolarizing (sufficiently well) the cell ferroelectric during the write-back step. As shown in Figure 3, an L is written back to a cell by simply driving the BL to 0 V while the PL is driven to $+V_{DD}$. An H is written back to a cell when the PL is driven back to 0 V while the BL is held at $+V_{DD}$. Writing the M level would be a more complex operation. To fully erase the previous cell state, another important challenge, one would first drive the BL to 0 V while the PL is driven to $+V_{DD}$ (as when writing back an L). Then the PL would be allowed to switch back to 0 V with the BL held at 0 V. Finally, the BL would need to be driven to a coercive voltage $+V_M$, such that $|V_M| < V_{DD}$. $V_M$ would be sized to be just large enough to produce a zero remanent polarization after the BL voltage is reduced back to 0 V.

The BL circuitry would thus be required to drive three voltages: 0 V, $+V_{DD}$ and $+V_M$. The first two drive voltages require transistor switches to the two low-impedance power supply nodes. $V_M$ could be provided by a regulated third supply voltage, or it could be provided by a feedback-stabilized analog amplifier powered by $V_{DD}$. This driver would require feedback to ensure that an accurate $V_M$ is produced on BL for all of the possible data-dependent cell loads. The cell load will vary depending on how many cells in the accessed row need to be written back with an M.

Figure 6 shows the paths traced through the hysteresis loop when the three possible levels are written. Figure 6(a) shows how an L is written starting from all three possible initial states. Figure 6(b) shows how an H is written. Finally, Figure 6(c) shows how an M is written. Note that the steepness of the hysteresis characteristic at the horizontal intercepts (i.e., at the coercive voltages) implies that errors in $V_M$ can cause significant errors in the final remanent polarization (which ideally should be zero).

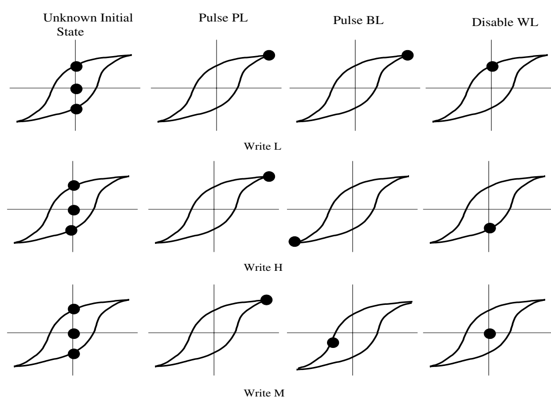


Fig. 6 Write Operations in Ternary FeRAM

Read operations in a ternary FeRAM can be accomplished using either serial or parallel sensing with respect to two reference bitline voltages, $V_{REF_H}$ and $V_{REF_L}$. $V_{REF_L}$ is located between the distributions of the L and M signals whereas $V_{REF_H}$ is located between the distributions of the M and H signals. In serial sensing, the cell signals are first compared against $V_{REF_L}$, and then afterwards compared with $V_{REF_H}$ (or vice versa). In parallel sensing, two copies must be made of each cell signal, and then the copies compared simultaneously against $V_{REF_L}$ and $V_{REF_H}$. Serial sensing allows the same sense amplifiers to be used in both sensing steps, at the cost of a longer read operation. Generation of suitable $V_{REF_L}$ and $V_{REF_H}$ signals in a ternary FeRAM would be comparable in difficulty to the generation of the $V_{REF}$ signal in a conventional binary FeRAM [1].

One complication in sensing is the need to create multiple copies of each cell signal in the case of destructive sensing with regenerative feedback (the typical case with conventional sense amplifiers). An approach that has been used successfully in multilevel DRAM is to create the copies of the cell signal by partitioning each bitline into two or more equal-capacitance subbitines [6, 7]. In the case of ternary FeRAM, the cell charge could first be dumped onto two connected subbitlines, then the two copies of the cell signal could be created by opening a transistor switch.

## 4. Modeling Parameter Variations

Among the principal challenges faced by ternary FeRAM are to ensure the accurate writing of the three signal states, as well as the reliable sensing of those cell states, despite the presence of the device parameter variations that are inevitably introduced during production. The situation is complex since many different parameters are involved, and accurate parameter distribution data is not publicly available. To permit our preliminary feasibility study, we relied upon the Central Limit Theorem and assumed that many of the various parameter variations can be combined to produce a normally-distributed scatter in an effective cell capacitor size. Our goal was then to determine how tightly the total variance on the effective cell size must be controlled to ensure sufficiently large noise margins on the BL signals for reliable sensing (e.g., at least 100 mV).

We used the ferroelectric capacitor model developed by Rickes [10] and assumed (for our convenience) the 0.35-μm CMOS logic process from Taiwan Semiconductor Manufacturing Corporation (TSMC). Rickes' model requires several parameters to be set. For example, to produce the plot in Figure 5 we set the cell area $A = 0.65$ $\mu m^2$, the PZT ferroelectric thickness $d = 170$ nm, the relative dielectric constant $\varepsilon_R = 350$, the saturation polarization $Ps = 30$ $\mu C/cm^2$, the remanent polarization $Pr = 25$ $\mu C/cm^2$, the positive coercive voltage $V_{CP} = 1.5$ V, the negative coercive voltage $V_{CN} = -1.5$ V, and the leakage resistance per unit capacitor area $R_{leak} = 5$ $K\Omega/cm^2$. These values, as well as the process parameters, could always be adjusted to suit any actual process.

A plot like the one in Figure 5 is obtained by first determining the relationship between the BL signal and the cell size starting with the cell in the L, M and H states. The


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plot in Figure 7 was obtained by simulating a cell capacitor plus bitline circuit (as in Fig 2(a)) using the same cell model parameters as above and assuming a typical bitline capacitance of 300 fF. The cell area is swept over a large range about the nominal value so that the resulting cell signal distribution can be constructed out into the tails.

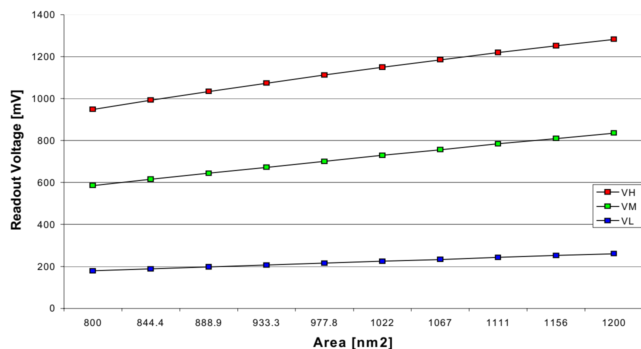


Fig. 7 BL Voltage versus Cell Area

Once the BL voltage versus cell size function is obtained for the given circuit configuration, a cell size variance is selected for the assumed normal distribution of effective cell sizes. For example, in the case of the plots in Figure 5 we assumed a cell size variance of 10%. An unnormalized probability density function (PDF) is obtained for a given signal level (L, M or H) by mapping a sequence of cell sizes into the corresponding sequence of BL signals. The same sequence of cell sizes is also associated with a sequence of probability density values from the normal distribution, as determined by the cell size variance. An unnormalized PDF of cell signals is then obtained by plotting the probability density values against the corresponding BL signal values. The resulting bell-shaped curve must then be normalized by scaling the points along the vertical direction in such a way that the area under the curve becomes unity. One such PDF curve is obtained for each of the three possible cell signals.

## 5. Some Results of the Simulation Study

Many different aspects of ternary FeRAM operation can be studied using the technique described in the preceding section [5]. For example, Figure 8 shows the PDFs for the same circuit configuration assumed for the plots in Figure 5 except that the cell variance has been increased from 10% to 20%. Clearly the tails of the three PDFs have begun to overlap, implying that the noise margins have disappeared and that sensing errors will be frequent. One could thus conclude that if that the manufacturing process must be capable of producing cells with effective areas with a variance of not much more than 10%. A cell size variance of 20% would make reliable ternary FeRAM operation impossible (but perhaps binary operation might still be acceptable).

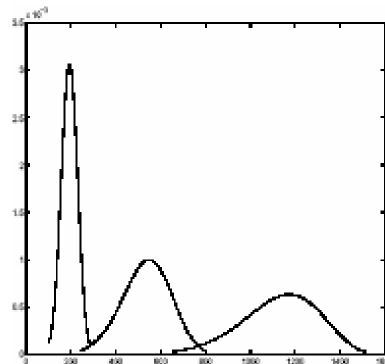

Fig. 8 BL Signal PDFs with 20% Cell Size Variance

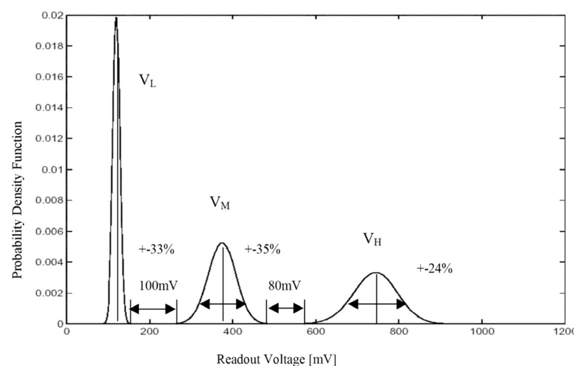


Fig. 9 BL Signal PDFs with 8% Cell Size Variance

Figure 9 shows the results of a simulation study in which the nominal cell size was set to 0.25 $\mu m^2$ and 8% variance in the effective cell size. The noise margin between the L and M distributions is about 100 mV, which was greater than the 80 mV noise margin between the M and H distributions. If one were expecting an effective cell size variance of up to 8% in a particular process, then one might consider slightly reducing the generated $V_M$ voltage on the bitlines to better equalize the two noise margins among the three data signal distributions.



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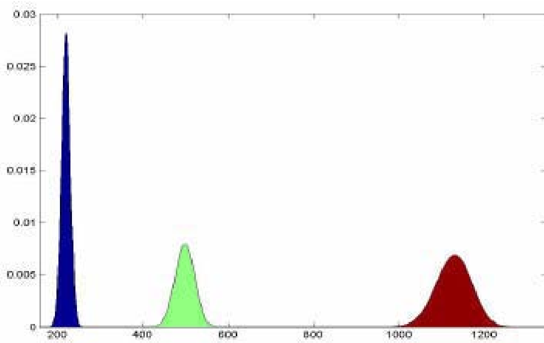


Fig. 10 BL Signal PDFs with $V_M$ 15% too low

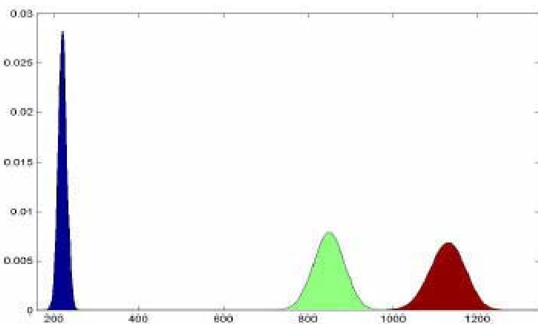


Fig. 11 BL Signal PDFs with $V_M$ 15% too high

We saw earlier that the accuracy of the M level (nominally the depolarized condition) depends strongly on the choice of the $V_M$ voltage. This is because the slope of the ferroelectric polarization characteristic is relatively steep as it passes zero polarization (i.e., at the coercive voltages). It is thus important to study the implications of the inevitable variations in $V_M$ as well as the cell characteristics on ternary FeRAM operation. Figures 10 (and 11) show how the M signal PDF is shifted downward (upward) when the $V_M$ voltage is 15% too low (15% too high) [5]. Errors $V_M$ on the positive side appear to be more problematic than errors on the negative side.

## 6. Conclusions

This paper investigated the practicality of three-level FeRAM operation in the presence of device parameter variations to better understand the feasibility of one possible way of increasing FeRAM storage density. In our simulation-based study the parameter variations were modeled as normally-distributed cell size variations. The maximum tolerable variance in equivalent cell size depends on the required minimum noise margins. To achieve noise margins of 100 mV, our simulations suggest that the effective cell size, taking into account all of the related device parameter variations, must be no more than about 8%. This would likely be a tough goal to achieve.

Several strategies could be considered to make ternary FeRAM more practical. For example, the choice of PZT is appropriate for binary FeRAM because of the relatively square hysteresis characteristic. However, PZT may not be the best ferroelectric material to use in a ternary FeRAM. A ferroelectric with a less steep characteristic at the coercive voltages (e.g., strontium bismuth tantalite, SBT) would make the FeRAM less sensitive to errors in the coercive voltage $V_M$ that is used to create the depolarized state (but this would also reduce the strength of the L and H signals).

With a suitable device architecture, it should be possible to design a ternary FeRAM in such a way that, if the cell yield in full ternary operation is too low, the same device can be reconfigured for more robust binary FeRAM operation. Perhaps this reconfiguration could be done on a per row basis instead of for subarrays or for the full memory array. In this way the risk of introducing a ternary FeRAM into production would be reduced.

There are many aspects of ternary FeRAM that need to be investigated more fully. The source of the $V_M$ signal is a critical element in the design. In [5] we investigated several possible $V_M$ driver designs that, for lack of space, could not be included in this paper.

## Acknowledgements

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## References

[1] A. Sheikholeslami and P. G. Gulak, "A survey of circuit innovations in ferroelectric random-access memories," *Proc. IEEE*, vol. 88, pp. 667-689, May 2000.

[2] Y. Chung, "Experimental 128-kbit ferroelectric memory with $10^{12}$ endurance and 10-year data retention," *IEE Proc-Circuits Devices Syst,* vol. 149, no. 2, April 2002.

[3] S. Sommerfelt et al., "Embedded Ferroelectric Memory Using a 130-nm 5 Metal Layer Cu / FSG Logic Process," *Fifth Annual Non-Volatile Memory Technology Symposium*, Nov. 14-17, 2004, Orlando, FL, USA, paper E-4.

[4] Fujitsu, 1-Mb FeRAM datasheet.

[5] K. R. Raiter, "Evaluation of a Three-level FeRAM," M.Sc. thesis, Department of Electrical and Computer Engineering, University of Alberta, Fall 2004.

[6] Y. Xiang et al., "Design of a Multilevel DRAM With Adjustable Cell Capacity, *Cdn. J. Electrical and Comp. Eng*., vol. 26, no. 2, Apr. 2001, pp. 55-59.

[7] J. Koob et al., "Test and Characterization of a Variable-Capacity Multilevel DRAM," *2005 IEEE VTS*.

[8] B. Jeon et al., "A 0.4-µm 3.3-V 1T1C 4-Mb nonvolatile ferroelectric RAM with fixed bitline reference voltage scheme and data protection circuit," *IEEE JSSC*, vol. 35, no. 11, pp. 1690-1694, November 2000.

[9] T. Chandler, A. Sheikholeslami, S. Masui and M. Oura, "An adaptive reference generation scheme for 1T1C FeRAMs," in *Symp. VLSI Circuits*, June 2003, pp. 173-174.

[10] J. T. Rickes, "Circuit Design of Gigabit Density Ferroelectric Random Access Memory," PhD dissertation, Rheinland-Westphalia Technical University, Dec. 2002.


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