



Research note

Back gate bias method of threshold voltage control for the design of low voltage CMOS ternary logic circuits

A. Srivastava *

Department of Electrical and Computer Engineering, Louisiana State University, South Campus Drive, Baton Rouge, LA 70803-5901, USA

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Abstract

Key building blocks – simple ternary inverter, positive ternary inverter and negative ternary inverter have been designed for operation at a low voltage – ± 1 V in $2\ \mu\text{m}$, n-well standard CMOS process and simulated in SPICE3 for use in the design of ternary logic circuits. The back-gate bias method has been used in conjunction with the width/channel (W/L) ratio of MOSFETs to generate the desired dc voltage transfer characteristics and transition region adjustment around midway between high and low logic levels. © 2000 Elsevier Science Ltd. All rights reserved.

1. Introduction

There are several techniques which are currently being exploited for the design of low-power digital circuits for varied applications. Some of these logic design techniques are based on adiabatic switching [1], automated low-power techniques exploiting multiple supply voltages [2], and dynamic threshold voltage control by biasing the bulk CMOS wells [3]. Basically, high-speed and low-power operation of digital circuits could be achieved by reducing both the power supply voltage, V_{DD} and threshold voltage, V_T of MOSFETs [4,5].

The supply voltage reduction is the commonly used technique in reducing power dissipation in CMOS circuits since static power dissipation is directly related to the V_{DD} and dynamic power dissipation is quadratically related to V_{DD} [6]. Dynamic power dissipation is the dominant component of the total power dissipation and can be significantly lowered by reducing the V_{DD} . However, the delay increases as V_{DD} is reduced, and reducing the threshold voltage with reducing V_{DD} increases the subthreshold current. Hence, it becomes essential to tradeoff between the power supply voltage and

threshold voltage for optimum circuit performance. The back-gate bias scheme has been used as a tradeoff between speed and subthreshold power [7–9]. The method of back-gate forward bias suitable for standard bulk CMOS process is being promoted for circuit level designs for low-voltage digital applications [10]. Heung and Mouftah [11] reported the design of three-valued logic circuits in non-standard CMOS processes. Recently, Srivastava and Venkatapathy [12] have designed ternary logic circuits and implemented them in $2\ \mu\text{m}$, n-well standard CMOS process for operation below ± 2 V. The ternary functions were implemented mainly by adjusting W/L ratios of transistors in a CMOS inverter and by using a transmission gate at the output. In the present work, it is shown through SPICE [13] simulation that the back-gate bias provides an additional parameter in the design of CMOS ternary logic circuits for the low-voltage operation at ± 1 V, where an adjustment of the transition region in voltage transfer characteristics for the switching threshold becomes crucial to designs.

2. Principle of the method

The following is the design equation of threshold voltage V_T of a MOSFET in CMOS circuits [14]:

* Tel.: +1-225-388-5241; fax: +1-225-388-5200.
E-mail address: ashok@ee.lsu.edu (A. Srivastava).

$$V_T = V_{T0} \pm \gamma \left(\sqrt{|-2\phi_F + V_b|} - \sqrt{2|\phi_F|} \right), \quad (1)$$

where V_{T0} is the zero-biased threshold voltage, γ is the body-effect coefficient, V_b is the back-gate bias, and $2|\phi_F|$ is the surface potential. The increase or decrease in V_T depends on the magnitude of V_b – reverse or forward biased. In dc voltage transfer characteristics of a CMOS inverter, the transition region adjustment at the midway between the high- and low-logic levels depends primarily on the W/L ratios of n- and p-channel MOSFETs. A better control of the transition region can be obtained by electrically adjusting the threshold voltage of MOSFETs since the turn-on and turn-off points on voltage transfer characteristics depend on the threshold voltage of MOSFETs. The back-gate bias could be used more effectively in the design of ternary logic circuits, where an additional design parameter is needed [12].

Three types of ternary operators are defined by [11]

$$\bar{X}_C = \begin{cases} C & \text{if } X = 1, \\ 2 - X & \text{if } X \neq 1. \end{cases} \quad (2)$$

C in Eq. (2) takes the value of logic 2 for PTI, logic 1 for STI and logic 0 for NTI which corresponds to higher (1), middle (0) and lower levels (–1), respectively. Figs. 1–3 show the schematics of STI, PTI and NTI, respectively. In Fig. 1, for STI, a CMOS transmission gate is connected to the common drain output of a CMOS inverter. In Fig. 2, for PTI, a p-MOSFET is connected to the output of a CMOS inverter. In Fig. 3 for NTI, an n-MOSFET is connected to the output of a CMOS inverter. The substrate bias connection in MOSFETs of the CMOS inverter is used to apply forward or reverse bias voltage, V_b , for the control of threshold voltage according to Eq. (1) and to adjust the transition region in dc voltage transfer characteristics.

The circuit diagrams in Figs. 1–3 for STI, PTI and NTI, respectively, can be implemented in standard dual

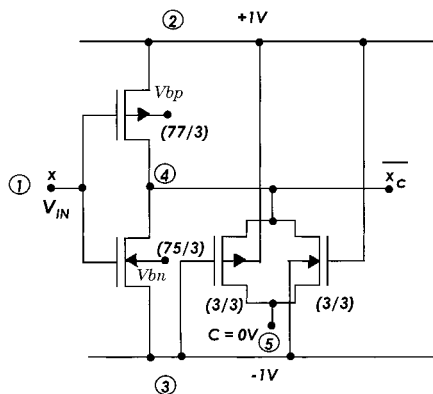


Fig. 1. Simple ternary inverter.

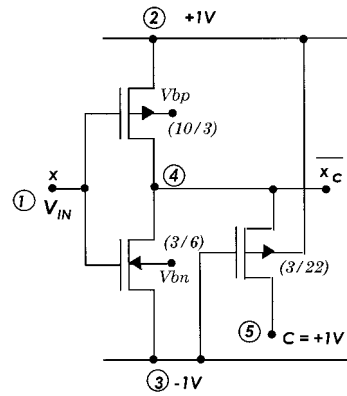


Fig. 2. Positive ternary inverter.

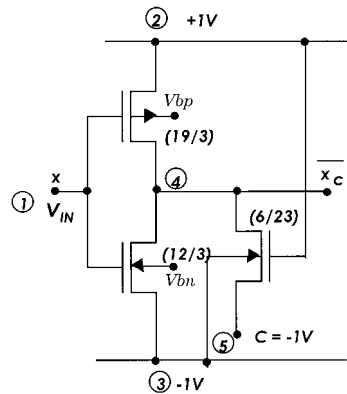


Fig. 3. Negative ternary inverter.

well CMOS processes using the p-substrate. These wells can be held either at the same potential or at different potentials. Thus, the use of a standard dual well CMOS process would allow us to apply different back gate biases in MOSFETs of ternary logic circuits. This would also eliminate the problem of the p-substrate becoming common for all n-MOSFETs in a typical n-well CMOS process. Part of the circuits in Figs. 1–3 uses either a transmission gate or a pass transistor, where the substrate for the p-MOSFET is connected to the most positive potential, and the substrate for the n-MOSFET is connected to the most negative potential.

3. Results and discussion

In the design of STI, PTI and NTI, the back-gate forward bias was not allowed to exceed beyond 0.4 V in order to avoid the CMOS latch-up condition. The ter-

nary circuits were designed in 2 μm , n-well standard CMOS process and simulated using the following SPICE Level 2 MOSFET model parameters [15]:

n-MOSFET model parameters: $V_{TO} = 0.7339$, $UO = 610.5$, $TOX = 4.12E-08$, $NSUB = 4.923E+15$, $XJ = 0.20U$, $LD = 2.356E-07$, $CGSO = 2.9620E-10$, $CGDO = 2.9620E-10$, $CJ = 1.3611E-04$, $MJ = 6.3320E-01$, $GAMMA = 0.4823$.

p-MOSFET model parameters: $V_{TO} = -0.7776$, $UO = 197.2$, $TOX = 4.12E-08$, $NSUB = 9.5750E+15$, $XJ = 0.20U$, $LD = 3.307E-07$, $CGSO = 4.1576E-10$, $CGDO = 4.1576E-10$, $CJ = 3.1861E-04$, $MJ = 6.0597E-01$, $GAMMA = 0.6727$.

Fig. 4 shows the dc voltage transfer characteristics of PTI and NTI for operation at ± 1 V with and without back-gate bias. The voltage transfer characteristics for PTI with back-gate bias corresponds to 0.15 V reverse bias for n-MOSFET and 0.15 V forward bias for the p-MOSFET. Similarly, the transition region of the voltage transfer characteristics in NTI was adjusted with 0.20 V back-gate reverse bias for n-MOSFET and 0.20 V back-gate forward bias for p-MOSFET. In Fig. 4, PTI and NTI characteristics have also been compared with $|0.3|$ V MOSFET's threshold voltage. Voltage transfer characteristics of PTI shows good improvement in comparison to the voltage transfer characteristics obtained with nearly $|0.73|$ V MOSFET's threshold voltage. However, no change in the voltage transfer characteristics of NTI is observed. Fig. 5 shows dc voltage transfer characteristics for an STI. It was mentioned in Ref. [12] that significant adjustment in V_T is needed to generate the functional transfer characteristics for a STI. No back-gate bias curve corresponds to $V_T = |1.5|V$ [12]. With back-gate bias, the threshold voltage of MOSFETs has

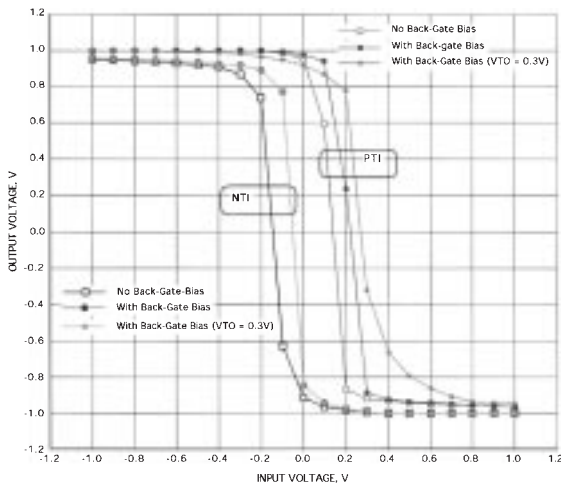


Fig. 4. Voltage transfer characteristics of PTI and NTI with and without back-gate bias.

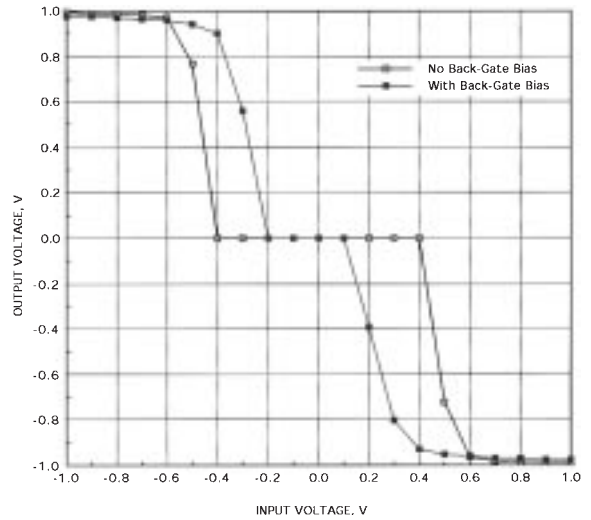


Fig. 5. Voltage transfer characteristics of a STI with and without back-gate bias.

been reduced to $|1|V$ – a value typically used in CMOS designs.

4. Conclusion

Ternary logic circuits – STI, PTI and NTI have been designed for operation at ± 1 V power supply voltage by adjusting the W/L ratios of transistors in a CMOS inverter and using transmission gate at the output. In addition to the W/L ratio as a design parameter, the back-gate bias has been used to adjust the transition region in voltage transfer characteristics around the midway between high- and low-logic levels. The method could be used where location of transition region in voltage transfer characteristics is critical to ternary logic designs. The presented ternary circuits could be implemented in standard dual well CMOS processes and used in the design of adiabatic ternary CMOS logic circuits.

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