ICECS 2004

The 11th IEEE International Conference on Electronics, Circuits and Systems.

December 13 – 15, 2004

Tel Aviv, Israel

Conference Program

General Chair's Welcome Message

Dear Colleagues working in the Circuits and Systems field – welcome to Israel!

This is the 11th IEEE International Conference on Electronics, Circuits and Systems, held for the first time in Tel-Aviv. ICECS has started out in the warm climate of the Middle East (Egypt), and is continuing in Tel-Aviv as an IEEE-CAS venue providing a welcome respite from the cold European winter along the balmy Mediterranean shores.

Thanks to the efforts of many around the world, we are able to offer a rich, high quality technical program spread over three days. We have invited three plenary keynote speakers, two from the academia and one from the industry. The keynote topics will provide a fascinating overview of circuits and systems in different fields. In addition, several special sessions have been organized on topics that have recently attracted attention, ranging from nano-scale technology to grand challenges in different circuits and systems fields. Also on the agenda are 6 half-day tutorials covering a wide range of topics: Operational Amplifiers, Analog Circuit Design Methodology. Video Processing. CMOS Imagers, the MOS Transistor, Computer Vision, and SOI CMOS.

The organization of an international conference is a major effort and requires the input, creativity and energy of many people. My thanks go to the Technical Program Committee Chair and members, to our conference manager and the people at the VLSI Systems Center at the Ben-Gurion University, who worked on the tasks at hand on a daily basis and learned a great deal about all the issues involved in organizing such international venue.

Our conference manager has arranged a very attractive social program that starts with a welcome reception on Sunday evening. You will get a taste of Tel-Aviv's history on Monday evening during the visit to the "white city" - as Tel Aviv was proclaimed by UNESCO in its list of world cultural heritage sites. On Tuesday evening the banquet dinner will take place with special guests of honor. In addition, you are invited to join us every evening for the Hanukah Candles lighting – a Jewish tradition performed during the Hanukah Holiday, the "Holiday of Lights", which takes place these days.

The IEEE Circuits and Systems Society provided overall sponsorship for the conference, and I thank them for their support. Additionally, I would like to thank our industrial partners: Freescale Semiconductors, Tower Semiconductor Ltd., IBM Israel, Orbotech and Intel Israel, for their generous sponsorship of this event.

We can certainly say that this conference offers a unique forum for researchers and practitioners from academia, industry and government to share their expertise, results, and achievements in all areas of circuits and systems.

Many individuals have contributed to the success of this conference. My sincere thanks go to all authors including those whose papers were not included in the program. Many thanks go to the Technical Program Committee members and the reviewers, and to the Steering Committee members, who sacrificed their time to make this event a first-class conference. Special thanks go to Professor Eby Friedman, our Technical Program Chair, for his tireless work in finalizing this outstanding technical program. Thanks are due to Professor George Moschytz for his ongoing support throughout the different stages. My thanks go also to our conference secretary, Professor Aryeh Weiss and to our treasurer, Professor Yisroel Rotman for their help, and to Professor John Harris and Professor Peter Wu for their enthusiasm and energy driving the special sessions.
I would also like to especially acknowledge our conference manager, Tami Polna-Guata who put much effort in making this conference a big success, and to Rachel Mahluf-Zilberberg, Vered Nitzan and Ruslan Sergienko for their continuous work on it.
Last but not least, I would like to thank my loved ones who put up with me all this time…

Enjoy the conference!

Orly Yadid-Pecht
General chair, ICECS 2004

Conference Organization

Co-Organized by:

Ben-Gurion University of the Negev, Beer-Sheva, Israel
The VLSI Systems Center**,** Ben-Gurion University of the Negev, Beer-Sheva, Israel.

Sponsored by:

IEEE Organization

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Freescale Semiconductor Inc.

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The VLSI Systems Center**,** Ben-Gurion University, Beer-Sheva, Israel
Department of Electrical Engineering, University of Calgary, Alberta, Canada.

Technical Program Chair
Eby Friedman,
University of Rochester, Rochester, NY, USA.

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Aryeh Weiss,
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Technical Program Committee

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Session Chairs

C. F. Tai	ANALOG AMPLIFIERS
S. Engelberg	NONLINEAR CIRCUITS
A. Kolodny	INTERCONNECT MODELING
C. Y. Wu	SPECIAL SESSION: NANOELECTRONICS, NANOTECHNOLOGY, AND GIGA-SCALE SYSTEMS
I. Filanovsky	RF OSCILLATORS
A. I. Perez / D. Sadot	COMMUNICATION SYSTEMS
Y. Nemirovsky	CMOS IMAGING SENSORS
J. G. Harris	SPECIAL SESSION: NEUROMORPHIC SYSTEMS
G. S. Moschytz	ANALOG FILTERS
R. Holzer	SIGMA-DELTA MODULATORS
D. Allstot	HIGH PERFORMANCE INTEGRATED CIRCUITS

A. Baric / D. Foty	NEURAL NETWORKS
J. G. Harris	SPECIAL SESSION: GRAND CHALLENGES IN CIRCUITS AND SYSTEMS
T. Galambos	CONVERSION CIRCUITS
S. Greenberg	VIDEO AND MULTIMEDIA TECHNOLOGY
G. Robins	PROCESS AND DEVICE SIMULATION
R. Ginosar / A. Morgenshtein	BIOMEDICAL AND INDUSTRIAL APPLICATIONS
P. Schechner	POWER ELECTRONICS
I. Wagner / J. Shappir	MIXED-SIGNAL CIRCUITS
G. Robins	SYSTEM AND DEVICE MODELING
Y. Bar-Shlomo	CONTROL SYSTEMS AND APPLICATIONS
T. Galambos	ANALOG CIRCUITS AND APPLICATIONS
M. A. Lagunas	COMMUNICATION RECEIVERS
A. Baric / A. Kolodny	INTERCONNECT DESIGN
J. G. Harris / R. Shavit	MICRO-OPTO-ELECTRO-MECHANICAL SYSTEMS

Y. Betser	SOC DESIGN AND INTEGRATION
S. Greenberg /N. Intrator	IMAGE AND VISION SYSTEMS
Y. Rosenwaks	DESIGN FOR TESTABILITY AND RELIABILITY
H. Yeshurun	SPECIAL SESSION: RE-INVENTING METHODS AND TOOLS FOR NEXT-GENERATION CMOS DESIGN
M. Werner	HIGH PERFORMANCE ARCHITECTURES
R. J. Chen / H. Aharoni	DIGITAL SIGNAL PROCESSING
D. Lubzens	SEQUENTIAL SYNTHESIS METHODOLOGIES
A. Morgenshtein,	IMAGE PROCESSING
I. Yarom	ADVANCED SYNTHESIS AND VERIFICATION METHODOLOGIES
M. Ahmadi	VLSI CRYPTOLOGY
I. Filanovsky	LOW NOISE AMPLIFIERS AND ADAPTIVE PROCESSING

General Information

Registration Desk

Hours: Saturday: 14:00 – 17:00
Sunday: 8:00 – 17:00
Monday: 8:00 – 18:30
Tuesday, Wednesday: 7:30 – 18:30

ICECS 2004 Secretariat e-mail: icecs2004@icecs2004.org

Message center
Message center will be situated at the Conference Registration Desk.

Internet center
Internet center access for e-mail will be available near the Registration Desk. It will consist of three internet computer positions and two connections to Laptops.

Preview Desk
Preview Desk is located at the Internet center and will be accessible during registration hours. Authors are requested to hand over their presentations, on CD or Disk on key in advance, in order to arrange their presentation automatically.

Proceeding CD-ROM
Conference registrants can purchase extra copies of the Proceeding CD-ROM at the Registration Desk.

Services
We have arranged some services for your convenience: Those services should be purchase in advance.
Lunch coupons at special conference rate, for the hotel restaurant are available at the conference registration desk.
Parking vouchers, for "Kikar Atarim" parking lot can be purchased from the Bellboy desk, at the hotel entrance (25 NIS per day).

Tourist Information Desk
Tourist Information Desk will be operated next to the Conference Registration Desk.

Social Program

Welcome Reception
Sunday, Dec. 12, 20:00- 21:30, "Yarden" Hall, Sheraton Moriah Hotel.

An Evening Tour in Rothschild Boulevard:
Monday, Dec.13, 19:00 - 21:00

This tour includes stories about the buildings in the boulevard and the people who lived in them. We'll also find a bit of nostalgia from Little Tel Aviv, and will visit the Independence Hall, where the State of Israel was proclaimed, courtesy of the Association for Tourism of Tel Aviv-Jaffa.

Everyone is welcome to join free of charge.
Departure from Sheraton Moriah Hotel lobby.

Banquet Dinner & Best paper award presentation.
Tuesday, Dec.14, 19:45 - 22:30, "Yarden" Hall, Sheraton Moriah Hotel.

16 of December 2004

16 of December 2004
Program of Optional Tours
ICECS 2004 organizers have arranged four interesting excursions that will best present the beauties of Israel:

Tour No. 1 Jerusalem of Gold - 12 or 16 of December

Tour No. 2 Massada National Park and the Dead Sea - 12 of December

Tour No. 3 The Sorek Cave & Mini Israel - 16 of December

Tour No. 4 The City of Caesarea and Haifa - 16 of December

Note! The tours will take place only if there are a minimum number of participants. The organizers reserve the right to cancel a given trip if the number of registrants is low, in which case the trip registration fees will be refunded in full.

Sunday, December 12

Tutorial

Morning Tutorial
Time: 9:00 – 12:30
Hall: Carmel

Circuit Techniques for Operational Amplifier Speed and Accuracy Improvement: Analog Circuit Design with Structural Methodology

Vadim V. Ivanov - Texas Instruments, Inc

I. M. Filanovsky - University of Alberta, Canada

Afternoon Tutorial
Time: 13:30 – 17:00
Hall: Carmel

Mixed Analog/Digital Circuits in SOI CMOS
Andreas G. Andreou - Johns Hopkins University, Baltimore, USA

Reception

20:00 – 21:30
"Yarden" Hall
Sheraton Moriah Hotel

Monday, December 13

"Arbel & Tabor" Hall:
Opening Remarks
9:00 – 9:15

Technical program overview
9:15 – 9:30

Plenary session
9:30 – 10:30
From LC Filters to Filters-on a-Chip: A Technological Odyssey.
G. Moschytz, Bar-Ilan University, Israel, Swiss Federal Institute of Technology Zürich (ETH)

Hall: Galil

Monday: 11:00-12:40
MA1- ANALOG AMPLIFIERS
Chair: **C. F. Tai**, Taiwan University, Taipei, Taiwan

11:00
MA1.1
A NEW CONFIGURATION OF TWO-STAGE WIDE-BAND AMPLIFIER WITH MATCHED INPUT AND OUTPUT IMPEDANCES, *I. Filanovsky, **A. Sachko, **J. Long, *University of Alberta, Edmonton, Canada, TU Delft, Netherlands.

11:20
MA1.2
A BULK-DRIVEN CMOS OTA WITH 68 DB DC GAIN, J. Rosenfeld, M. Kozak, E. G. Friedman, University of Rochester, Rochester, NY, USA.

11:40
MA1.3
A 100 DB CMRR CMOS OPERATIONAL AMPLIFIER WITH SINGLE-SUPPLY CAPABILITY, I. Filanovsky, V. Ivanov, J. Zhou, University of Alberta, Edmonton, Canada

12:00
MA1.4
TWO NOVEL CROSS-CASCODE DIFFERENTIAL AMPLIFIERS, Y. Bruck, M. Zelikson, IBM, Haifa, Israel.

12:20
MA1.5
A WIDE-LINEAR RANGE SUBTHRESHOLD OTA BASED ON FGMOS TRANSISTOR, A. El Mourabit, P. Pittet, G. N. Lu, University of Claude Bernard, Lenac, France.

Monday: 14:00-15:40
MA2: RF OSCILLATORS
Chair: **I. Filanovsky**, University of Alberta, Canada**.**

14:00
MA2.1
**A 6GHZ LOW-NOISE QUADRATURE COLPITTS VCO, ***M. Chu, D. Allstot, University of Washington, Seattle, WA, USA.

14:20
MA2.2
DESIGN CONSIDERATIONS FOR ANTI-PHASE INJECTED QUADRATURE VOLTAGE CONTROLLED OSCILLATORS, *****M. Chu, *****S. Shekhar, *****D. Allstot, ******T. Bhattacharyya, *****University of Washington, Seattle, Washington, USA, ******Indian Institute of Technology, Kharagpur, India**.**

14:40
MA2.3
A MULTI-TANK LC-OSCILLATOR, C. Samori, L. Romano, S. Levantino, A. Bonfanti, A. Lacaita, Polytechnic of Milan, Milan, Italy.

15:00
MA2.4
DIFFERENTIAL TUNING OSCILLATORS WITH REDUCED FLICKER NOISE UPCONVERSION, C. Samori, S. Levantino, A. Bonfanti, L. Romano, A. Lacaita, Polytechnic of Milan, Milan, Italy.

15:20
MA2.5
ANALYSIS AND DESIGN OF A DUAL BAND RECONFIGURABLE VCO, *A. Mazzanti, **P. Uggetti, **R. Battaglia, **F. Svelto, *University of Modena e Reggio Emilia, Modena, Italy, **University of Pavia, Pavia, Italy.

Monday: 16:00-17:40
MA3: ANALOG FILTERS
Chair: G. S. **Moschytz**, Bar-Ilan University, Israel.

16:00
MA3.1
DYNAMIC RANGE, NOISE AND LINEARITY OPTIMIZATION OF CONTINUOUS-TIME OTA-C FILTERS, *S. Koziel, **A. Ramachandran, *S. Szczepanski, **E. Sanchez-Sinencio, Gdansk *University of Technology, Gdasnk, Poland, **Texas A&M University, College Station, TX, USA.

16:20
MA3.2
NOISE ANALYSIS AND OPTIMIZATION OF CONTINUOUS-TIME ACTIVE-RC FILTERS, S. Koziel, Gdansk University of Technology, Gdasnk, Poland.

16:40
MA3.3
GENERAL ACTIVE-RC FILTER MODEL FOR COMPUTER-AIDED DESIGN AND OPTIMIZATION, S. Koziel, Gdansk University of Technology, Gdasnk, Poland.

17:00
MA3.4
A NOVEL METHOD FOR THE CLOSED-FORM ANALYSIS AND DESIGN OF A 4THORDER SINGLE-AMPLIFIER FILTER, *D. Jurisic, N. Mijat, **G. S. Moschytz, *University of Zagreb, Zagreb, Croatia, **Institute of Technology, Zurich, Switzerland, **Bar-Ilan University, Ramat-Gan, Israel**.**

17:20
MA3.5
ANALYSIS OF LINEAR SYSTEM RESPONSE TO WIDE BAND SIGNALS WITH APPLICATIONS TO FILTERS, A. Yahalom, Y. Pinhasi, The College of Judea and Samaria, Ariel, Israel.

Hall: Carmel

Monday: 11:00-12:40
MB1: NONLINEAR CIRCUITS
Chair: **S. Engelberg**, Jerusalem College of Technology, Israel.

11:00
MB1.1
NONLINEAR DYNAMICS OF FIRST-ORDER DPLL WITH FM INPUT AND PHASE DETECTOR DC OFFSET, B. O'Donnell, P.I. Curran, University College Dublin, Dublin, Ireland.

11:20
MB1.2
THE CENTRAL LIMIT THEOREM AND LOW-PASS FILTERS, S. Engelberg, Jerusalem College of Technology - Machon Lev, Jerusalem, Israel.

11:40
MB1.3
MATHEMATICAL PROGRAMMING AND RESISTOR TRANSFORMER DIODE NETWORKS, N. Harihar, IIT Bombay, Mumbai, India.

12:00
MB1.4
A NEW METHOD TO IMPROVE THE IMPEDANCE OF THE CC-II'S X INPUT, L. N. Alves, R. Aguiar, University of Aveiro, Aveiro, Portugal.

12:40
MB1.5
NEW CHAOTIC THIRD-ORDER LOG-DOMAIN OSCILLATOR WITH TANH NONLINEARITY, A. Ascoli, P. Curran, O. Feely, University College Dublin, Dublin, Ireland.

Monday: 14:00-15:40
MB2: COMMUNICATION SYSTEMS
Chair: **A. I. Perez Neira**, CTTC, Barcelona, Spain / **D. Sadot**, Ben-Gurion University, Beer-Sheva, Israel.

14:00
MB2.1
A UNIFIED FAIRNESS FRAMEWORK IN MULTI-ANTENNA MULTI-USER CHANNELS, D. Bartolome, A. I. Perez-Neira, Telecommunications Technological Center of Catalonia (CTTC), Barcelona, Spain.

14:20
MB2.2
ERGODIC CAPACITY OF A 2X2 MIMO SYSTEM UNDER PHASE UNCERTAINTY AT THE TRANSMITTER, M. Payaro, X. Mestre M. A. Langunas, Telecommunications Technological Center of Catalonia (CTTC), Barcelona, Spain.

14:40
MB2.3
ANALYSIS OF THE PROBABILITY DISTRIBUTION OF THE BASELINE WANDER EFFECT FOR BASEBAND PAM TRANSMISSION WITH APPLICATION TO GIGABIT ETHERNET, N. Sommer, I. Lusky, M. Miller, Texas Instruments, Herzlia, Israel.

15:00
MB2.4
VIRTUAL INPUT QUEUED PACKET SWITCHES WITH NON-UNIFORM ARRIVALS AND BURSTY SERVICE, I. Elhanany, M. Kahane, O. Arazi, University of Tennessee, Knoxville, TN, USA.

15:20
MB2.5
PERFORMANCE EVALUATION OF PSEUDO SELF-SIMILAR TRAFFIC, M. Kahane, Y. Ben-Shimol, D. Sadot, Ben-Gurion University, Beer-Sheva, Israel.

Monday: 16:00-17:40
MB3: SIGMA-DELTA MODULATORS
Chair: **R. Holzer**, AD, Herzelia, Israel.

16:00
MB3.1
AN IF INPUT CONTINUOUS-TIME SIGMA-DELTA ANALOG-DIGITAL CONVERTER WITH HIGH IMAGE REJECTION, J. Shen, K. Pun, C. Choy, C. Chan, The Chinese University of Hong Kong, Hong Kong.

16:20
MB3.2
A NOVEL SIGNAL-PREDICTING MULTIBIT DELTA-SIGMA MODULATOR, X. Lu, Concordia University, Montreal, Quebec, Canada.

16:40
MB3.3
A JITTER INSENSITIVE CONTINUOUS-TIME SIGMA-DELTA MODULATOR USING TRANSMISSION LINES, *L. Hernandez, **R. Pieter, *E. Prefasi, *S. Paton, *M. Garcia, *C. Lopez, *Universidad Carlos III de Madrid, Madrid, Spain, **Ghent University, Gent, Belgium.

17:00
MB3.4
A 250 MHZ DELTA-SIGMA MODULATOR FOR LOW COST ULTRASOUND/SONAR BEAMFORMING APPLICATIONS, B. Shem-Tov, M. Kozak, E. G. Friedman, University of Rochester, Rochester, NY, USA.

17:20
MB3.5
MULTIBIT DELTA-SIGMA CMOS DAC EMPLOYING ENHANCED NOISE-SHAPED DEM ARCHITECTURE, *D. Akselrod, **S. Greenberg, **S. Hava, *Motorola, Herzlia, Israel, **Ben-Gurion University, Beer-Sheva, Israel.

Hall Tabor

Monday: 11:00-12:40
MC1: INTERCONNECT MODELING
Chair: **A. Kolodny**, Technion, Haifa, Israel.

11:00
MC1.1
ELECTROMIGRATION-DEPENDENT PARAMETRIC YIELD ESTIMATION, *R. Barsky, **I. A. Wagner, *Technion, Haifa, Israel, **IBM, Haifa, Israel.

11:20
MC1.2
REPEATER INSERTION COMBINED WITH LGR METHODOLOGY FOR ON-CHIP INTERCONNECT TIMING OPTIMIZATION, M. Moreinis, A. Morgenshtein, I. Wagner, A. Kolodny, Technion, Haifa, Israel.

11:40
MC1.3
3D POWER GRID MODELING, Y. Yagil, L. Zlydina, Intel Corporation, Haifa, Israel.

12:00
MC1.4
PULSE-FORMING REACTANCE NETWORK SHAPES A QUASI-RECTANGULAR PULSE FROM SINUSOIDAL VOLTAGE, I. M. Filanovsky, X. Dong, University of Alberta, Alberta, Canada.

12:20
MC1.5
MODELING OF INTEGRATED MONOLITHIC TRANSFORMERS FOR SILICON RF IC, O. El Gharniti, E. Kerherve, J. B. Begueret, P. Jarry, University of Bordeaux, Bordeaux, France.

Monday: 14:00-15:40
MC2: CMOS IMAGING SENSORS
Chair: Y. Nemirovsky, Technion, Haifa, Israel.

14:00
MC2.1
A CMOS FOCAL-PLANE RETINAL SENSOR DESIGNED FOR SHEAR MOTION DETECTION, W. C. Hsieh, C. Y. Wu, C. T.Chiang, National Chiao Tung University, Hsing Chu City, Taiwan.

14:20
MC2.2
MORTON (Z) SCAN BASED REAL-TIME VARIABLE RESOLUTION CMOS IMAGE SENSOR, * **O. Yadid-, *E. Artyomov, *Y. Rivenson, **G. Levi, Ben-Gurion University, Beer-Sheva, Israel,** ** University of Calgary, Alberta, Canada.

14:40
MC2.3
LOW POWER GLOBAL SHUTTER CMOS ACTIVE PIXEL IMAGE SENSOR WITH ULTRA-HIGH DYNAMIC RANGE, *A. Fish, *A. Belenky, *, **O. Yadid-Pecht, VLSI System Center Ben-Gurion University, Beer-Sheva, Israel**, **** University of Calgary, Alberta, Canada.

15:00
MC2.4
CMOS APS PHOTORESPONSE AND CROSSTALK OPTIMIZATION ANALYSIS FOR SCALABLE CMOS TECHNOLOGIES, *I. Shcherback, *, **O. Yadid-Pecht, Ben-Gurion University, Beer-Sheva, Israel, University of Calgary, Alberta, Canada.

15:20
MC2.5
CMOS SOI IMAGE SENSOR, I. Brouk, Y. Nemirovsky, Technion, Haifa, Israel

Monday: 16:00-17:40
MC3: HIGH PERFORMANCE INTEGRATED CIRCUITS
Chair: **D. Allstot**, University of Washington, Seattle, USA.

16:00
MC3.1
IMPEDANCE CHARACTERISTICS OF DECOUPLING CAPACITORS IN MULTI-POWER DISTRIBUTION SYSTEMS, M. Popovich, E. G. Friedman, University of Rochester, Rochester, NY, USA

16:20
MC3.2
LOW ENERGY ASYNCHRONOUS ADDERS, I. Obridko, R. Ginosar, Technion, Haifa, Israel

16:40
MC3.3
TRAVELLING WAVE $LINBO_3$ ELECTRO-OPTIC MODULATOR WITH QUASI-PHASE-MATCH CPW STRUCTURE FOR TIME-DOMAIN APPLICATIONS, [*]O. V. Kolokoltsev, [**]S. V. Koshevaya, [*]R. A. Correa, [**]J. S. Alatorre, [**]M. A. Basurto-Pensado, [***]V. V. Grimalsky, , [*]National Autonomous University of Mexico, CD Universitaria, Mexico, [**]Autonomous State University of Morelos, Cuernavaca Mor., Mexico, [**]National Institute for Astrophysics, Optics, and Electronics (INAOE), Puebla, Mexico

17:00
MC3.4
NOISE CHARACTERIZATION OF THE 0.35UM CMOS ANALOG PROCESS IMPLEMENTED IN REGULATED AND SOI WAFERS, I. Brouk, Y. Nemirovsky, Technion, Haifa, Israel

17:20
MC3.5
A 0.8V CMOS TSPC ADIABATIC DCVS LOGIC CIRCUIT WITH THE BOOTSTRAP TECHNIQUE FOR LOW-POWER VLSI, H. P. Chen, J. B. Kuo, National Taiwan University, Taipei, Taiwan

Hall Arbel

Monday: 11:00-12:40
MD1: SPECIAL SESSION - NANOELECTRONICS, NANOTECHNOLOGY, AND GIGA-SCALE SYSTEMS.
Chair: **P. (Chung-Yu) Wu,** National Chiao Tung University**,** Taiwan.

11:00
MD1.1
A LOW POWER DESIGN ON DIFFUSIVE INTERCONNECTION LARGE-NEIGHBORHOOD CELLULAR NONLINEAR NETWORK FOR GIGA-SCALE SYSTEM APPLICATIONS, S. Chen, C. Y. Wu, National Chiao Tung University, Hsinchu, Taiwan

11:20
MD1.2
A LEARNABLE SELF-FEEDBACK RATIO-MEMORY CELLULAR NONLINEAR NETWORK (SRMCNN) WITH B TEMPLATES FOR ASSOCIATIVE MEMORY APPLICATIONS, [*,**]J. L. Lai, [**]C. Y. Wu, [*]National Chiao Tung University, Hsinchu, Taiwan, [**]National United University, Miao-Li, Taiwan

11:40
MD1.3
VLSI IMPLEMENTATION OF THE UNIVERSAL 2-D CAT/ICAT SYSTEM, R. J. Chen, J. L. Lai, National United University, Miao-Li, Taiwan

12:00
MD1.4
OPTIMAL STRUCTURE OF INTERCONNECTION LINES FOR GHZ GIGA-SCALE NANO-CMOS SYSYTEM-ON-CHIP DESIGN, [*]C. Y. Wu, [**]J. C. Wang, [*]National Chiao Tung University, Hsinchu, Taiwan, [**]Chip Implementation Center, National science Council, Hsinchu, Taiwan

12:20
MD1.5
SPINTRONIC LOGIC CIRCUIT DESIGN FOR NANOSCALE COMPUTATION, [*]J. Chen, [**]W.Chao, [**]Q.W. Shi, *Brown University, Providence, RI, USA, [**]University of Science and Technology, Beijing, China

Monday: 14:00-15:40
MD2: SPECIAL SESSION - NEUROMORPHIC SYSTEMS
Chair: **J. G. Harris**, University of Florida, FI, USA.

14:00
MD2.1
TOWARDS A SPIKING VLSI IMPLEMENTATION OF FREEMAN'S OLFACTORY MODEL, T. A. Holz, J. Harris, University of Florida, Gainesville, FL, USA.

14:20
MD2.2
A WINNER-TAKE-ALL NETWORK WITH SPIKING INPUTS, *M. Oster, *S. C. Liu, **J. Harris *Institute of Neuroinformatics, Zurich, Switzerland, **University of Florida, USA.

14:40
MD2.3
SPATIAL ACUITY MODULATION OF AN ADDRESS-EVENT IMAGER, *R. J. Vogelstein, *U. Mallik, *E. Culurciello, *R. Etienne-Cummings, *G. Cauwenberghs,**J. Harris, Johns Hopkins University, Baltimore, MD, USA, **UF,Florida, USA.

15:00
MD2.4
IMPROVED ON/OFF TEMPORALY DIFFERENTIATING ADDRESS-EVENT IMAGER, P. Lichtsteiner, T. Delbruck, J. Kramer, Institute of Neuroinformatics, ETH/University Zurich, Zurich, Switzerland.

15:20
MD2.5
ACTIVE PIXEL SENSOR WITH ON-CHIP NORMAL FLOW COMPUTATION ON THE
READ OUT, V. Gruev, R. Etienne-Cummings, Johns Hopkins University, Baltimore, MD, USA.

Monday: 16:00-17:40
MD3: NEURAL NETWORKS
Chair: **A. Baric**, University of Zagreb, Croatia **/ D. Foty**, Gilgamesh Associates, Fletcher, VT, USA.

16:00
MD3.1
SECURITY OF NEURAL CRYPTOGRAPHY, *R. Mislovaty, *E. Klein, *I. Kanter, **W. Kinzel, *Bar-Ilan University, Ramat-Gan, Israel, **Wurzburg University, Wurzburg, Germany.

16:20
MD3.2
TEXTURE BOUNDARY DETECTION BASED ON MULTIPLE AND PARALLEL CELLULAR NEURAL NETWORKS, C. H. Huang, C. T. Lin, National Chiao-Tung University, Hsin - Chu, Taiwan.

16:40
MD3.3
NEW CONDITIONS FOR EXPONENTIAL STABILITY OF DELAY IMPULSIVE NEURAL NETWORKS, Z. Yang, D. Xu, J. Deng, J. Niu, Sichuan University, Chengdu, Sichuan, China.

17:00
MD3.4
GLOBAL EXPONENTIAL STABILITY OF COHEN-GROSSBERG NEURAL NETWORKS WITH MULTIPLE TIME-VARYING DELAYS, J. Deng, D. Xu, Z. Yang, Mathematics College,
Sichuan University, Chengdu, China.

17:20
MD3.5
HIGH SPEED AND HIGH RESOLUTION CURRENT LOSER-TAKE-ALL CIRCUIT OF O(N) COMPLEXITY, *A. Fish, *V. Mirlud, *, **O. Yadid-Pecht, Ben-Gurion University, Beer-Sheva, Israel, University of Calgary, Alberta, Canada

Conference entrance hall

Lighting of the Hanuka candles
18:00 – 18:15

Tuesday, December 14

"Arbel & Tabor" Hall

Plenary session
8:00 – 8:55

Microprocessors: Bypass the power wall

(at least for a while)

Uri Weiser- Intel Corporation, Technion, Haifa, Israel

Tuesday: 9:00 – 10:40
TA1: SPECIAL SESSION - GRAND CHALLENGES IN CIRCUITS AND SYSTEMS
Chair: **J. G. Harris**, University of Florida, Gainesville, FL, USA.

Hall Galil

Tuesday: 9:00 – 10:40
TA1.1
CHALLENGES IN ULTRA DEEP SUBMICROMETER HIGH PERFORMANCE VLSI CIRCUITS, E. G. Friedman, University of Rochester, Rochester, NY, USA.

Tuesday: 11:00-12:40
TA2: CONVERSION CIRCUITS
Chair: **T. Galambos**, Intel, Haifa, Israel

11:00
TA2.1
HARDWARE-EFFICIENT PRBGS BASED ON 1-D PIECEWISE LINEAR CHAOTIC MAPS, T. Addabbo, M. Alioto, S. Bernardi, A. Fort, S. Rocchi, V. Vignoli, University of Siena, Siena, Italy.

11:20
TA2.2
AN AVERAGE LOW OFFSET COMPARATOR FOR 1.25 GSAMPLE/S ADC IN 0.18UM CMOS, N. Stefano, S. Sonkusale, Texas A&M University, College Station, TX, USA.

11:40
TA2.3
A 4GSPS, 2-4GHZ INPUT BANDWIDTH, 3-BITS FLASH A/D CONVERTER, C. Recoquillon, J. B. Begueret, Y. Deval, G. Montignac, A. Baudry, University of Bordeaux, Bordeaux, France.

12:00
TA2.4
A 10-B 500MSPS CURRENT-STEERING CMOS D/A CONVERTER WITH A SELFCALIBRATED CURRENT BIASING TECHNIQUE, M. Song, S. Hwang, University of Dongguk, Seoul, Korea**.**

12:20
TA2.5
SIGNAL PROCESSING BUILDING BLOCKS FOR PIPELINED A/D CONVERTER, R. Suszynski, K. Wawryn, B. Strzeszewski, Technical University of Koszalin, Koszalin, Poland.

Tuesday: 14:00-15:40
TA3: POWER ELECTRONICS
Chair: **P. Schechner**, Ort B. A. College of Engineering, Carmiel, Israel.

14:00
TA3.1
SHUNT VOLTAGE REGULATORS FOR AUTONOMOUS INDUCTION GENERATORS, PART I: PRINCIPLES OF OPERATION, A. Kuperman, R. Rabinovici, Ben-Gurion University, Beer- Sheva, Israel.

14:20
TA3.2
SHUNT VOLTAGE REGULATORS FOR AUTONOMOUS INDUCTION GENERATORS, PART II: CIRCUITS AND SYSTEMS, A. Kuperman, R. Rabinovici, Ben-Gurion University, Beer- Sheva, Israel.

14:40
TA3.3
HIGH-VOLTAGE TOLERANT WATCHDOG COMPARATOR IN A LOW-VOLTAGE CMOS TECHNOLOGY, V. Potanin, E. Potanina, National Semiconductor Corporation, Santa Clara, CA, USA.

15:00
TA3.4
A RESTRICTION ON THE POWER SYSTEM BY THEORETICAL REQUISITIONS OF THE BCU METHOD, N. Jiang, W. Song, Southeast University, Nanjing, China.

15:20
TA3.5
PERFORMANCE OF A GLUCOSE AFC, * L. Mor, ***** E. Bubis, ****** K. Hemmes, ***** P. Schechner, ***** Ort Braude Academic College of Engineering, Carmiel, Israel, ****** Delft University of Technology, Delft, the Netherlands.

Tuesday: 16:00-17:40
TA4: ANALOG CIRCUITS AND APPLICATIONS
Chair: **T. Galambos**, Intel, Haifa, Israel.

16:00
TA4.1
INPUT-FREE CASCODE VTHN AND VTHP EXTRACTOR CIRCUITS, *Y. Wang, *G. Tarr, **Y. Wang, *Carleton University, Ottawa, ON, Canada, **Concordia University, Montreal, Quebec, Canada.

16:20
TA4.2
FUZZY DECISION DIAGRAM REALIZATION BY ANALOG CMOS SUMMING AMPLIFIERS, *I. *Levin, **V. Varshavsky, *V. Marakhovsky, *A. Ruderman, *N. Kravchenko, * Bar Ilan University, Ramat-Gan, Israel, **The University of Aizu, Aizu-Wakamatsu, Japan.

16:40
TA4.3
A LOW-POWER ANALOG SPIKE DETECTOR FOR EXTRACELLULAR NEURAL RECORDINGS , C. L. Rogers, J. Harris, University of Florida, Gainesville, FL, USA.

17:00
TA4.4
A 2.4GHZ FULLY CMOS INTEGRATED RF TRANSCEIVER FOR 802.11B WIRELESS LAN APPLICATION, W. Kong, University of Maryland, College Park, MD, USA.

17:20
TA4.5
DESIGN OF A DIFFERENTIALL CHAOTIC COLPITTS OSCILLATOR, *O. Tsakiridis, **E. Zervas, ***D. Syvridis, ***M. Tsilis, *J. Stonham, *Brunel University Uxbridge, Middx, UK, **TEI-Athens, Athens, Greece, ***University of Athens, Athens, Greece.

Hall: Carmel

Tuesday: 9:00 – 10:40
TA1.2
GRAND CHALLENGES IN IMAGE PROCESSING AND ANALYSIS,
A. Bruckstein, Technion, Haifa, Israel.

Tuesday: 11:00-12:40
TB2: VIDEO AND MULTIMEDIA TECHNOLOGY
Chair: **S. Greenberg**, Freescale Semiconductor, Beer- Sheva, Israel

11:00
TB2.1
MULTISTAGE QUANTIZATION VIA CONDITIONAL HIERARCHICAL MAPPING, A. Eshet, M. Feder, Tel-Aviv University, Tel-Aviv, Israel.

11:20
TB2.2
RING-SHAPED N+/P -WELL PHOTODIODE: STUDY OF RESPONSIVITY ENHANCEMENT, *T. Danov, *I. Shcherback, *, **O. Yadid-Pecht, Ben-Gurion University, Beer-Sheva, Israel, University of Calgary, Alberta, Canada.

11:40
TB2.3
A HIGH PRECISION AND LOW NOISE S/H CIRCUIT DESIGN FOR VIDEO SIGNAL SAMPLING, *D. Xu, **X. Lai, **L. Hu, **H. Wang, *University of Teesside, Middlesbrough, UK, **Xidian University, Xian, China.

12:00
TB2.4
STENCIL SHADOW VOLUMES FOR COMPLEX AND DEFORMABLE OBJECTS, Z. Mihajlovic, I. Kolic, L. Budin, University of Zagreb, Zagreb, Croatia.

12:40
TB2.5
ALGORITHM FOR FACIAL WEIGHT-CHANGE, U. Danino, N. Kiryati, M. Furst, Tel- Aviv University, Tel-Aviv, Israel.

Tuesday: 14:00-15:40
TB3: MIXED-SIGNAL CIRCUITS
Chair: **I. Wagner**, IBM Haifa Labs, Haifa, Israel **/ J. Shappir**, Bar-Ilan University, Ramat-Gan, Israel

14:00
TB3.1
A SPIKE-BASED ADAPTIVE FILTER, X. Gong, J. Harris, University of Florida, Gainesville, FL, USA

14:20
TB3.2
A ROBUST OFFSET CANCELLATION SCHEME FOR ANALOG MULTIPLIERS, X. Wang, Z. Shi, S. Sonkusale, Texas A&M University, College Station, TX, USA.

14:40
TB3.3
SPARSE APPROXIMATIONS WITH A HIGH RESOLUTION GREEDY ALGORITHM, B. Salomon, H. Ur, Tel-Aviv University, Tel-Aviv, Israel.

15:00
TB3.4
A CPFSK/PSK-PHASE RECONSTRUCTION-RECEIVER FOR ENHANCED DATA RATE BLUETOOTH SYSTEMS, *D. Bruckmann, **M. Hammes, **A. Neubauer, *University of Wuppertal, Wuppertal, Germany, **Infineon Technologies, Dusseldorf, Germany.

15:20
TB3.5
A LOW COMPLEXITY COORDINATED FEXT CANCELLATION FOR VDSL, A. Leshem, L. Youming, Bar Ilan University, Ramat-Gan, Israel.

Tuesday: 16:00-17:40
TB4: COMMUNICATION RECEIVERS
Chair: **M. A. Lagunas**, CTTC, Barcelona, Spain

16:00
TB4.1
FAST ACQUISITION ARCHITECTURES FOR DIRECT-SEQUENCE SPREAD-SPECTRUM SYSTEMS, D. M. Frai, A. Reichman, Tel-Aviv University, Tel-Aviv, Israel.

16:20
TB4.2
ML ITERATIVE TENTATIVE-DECISION-DIRECTED (ML-ITDD): A CARRIER SYNCHRONIZATION SYSTEM FOR SHORT PACKET TURBO CODED COMMUNICATION, Y. Rahamim, A. Freedman, A. Reichman, Tel-Aviv University, Tel-Aviv, Israel.

16:40
TB4.3
TIMING RECOVERY OF PAM SIGNALS USING BAUD RATE INTERPOLATION, N. Sommer, Texas Instruments, Herzlia, Israel.

17:00
TB4.4
ANALYSIS OF LOCK-LOSS EVENTS IN DISCRETE-TIME PHASE LOCKED LOOP (PLL), L. Brecher, N. Sommer, E. Weinstein, Texas Instruments, Herzlia, Israel.

17:20
TB4.5
IMPLEMENTATION OF THE BERLEKAMP-MASSEY ALGORITHM USING DSP, S. Greenberg, N. Feldblum, G. Melamed, Motorola Semiconductor Israel, Omer, Israel.

Hall: Tabor

Tuesday: 9:00 – 10:40
TA1.3
CHALLENGES IN CMOS IMAGER DESIGN, O. Yadid-Pecht, VLSI System Center, Ben-Gurion University, Beer-Sheva, Israel, University of Calgary, Alberta, Canada.

Tuesday: 11:00-12:40
TC2: PROCESS AND DEVICE SIMULATION
Chair: **G. Robins**, University of Virginia, Charlottesville, VA, USA.

11:00
TC2.1
EXPERIMENTAL EXTRACTION OF POINT DEFECTS PARAMETERS NEEDED FOR 2-D PROCESS SIMULATION USING REVERSE MODELING, E. N. Shauly, G. Richard, Y. Komem, Tower Semiconductor, Migdal Ha'Emek, Israel**.**

11:20
TC2.2
ANALYSIS AND SIMULATION OF SPIRAL INDUCTOR FABRICATED ON SILICON SUBSTRATE, S. Yoshitomi, TOSHIBA Corp, Semiconductor Company, Yokohama, Kanagawa, Japan.

11:40
TC2.3
RAPID CAD PROTOTYPING FOR NANOTECHNOLOGY USING OBJECTIVE-C AND COCOA, A. K. Jones, B. Brady, I. Kourtev, University of Pittsburgh, Pittsburgh, PA, USA.

12:00
TC2.4
DESIGN OF WAVEGUIDING PHOTONIC BANDGAP DEVICES BY USING THE BLOCKFLOQUET THEOREM, A. G. Perri, A. Giorgio, R. Diana, Polytechnic of Bari, Bari, Italy**.**

12:20
TC2.5
EVALUATION OF THE NEW OASIS FORMAT FOR LAYOUT FILL COMPRESSION, *G. Robins, **A. Zelikovsky, ***Y. Zheng, *University of Virginia, Charlottesville, VA, USA, **Georgia State University, Atlanta, GA, USA, ***University of California, San-Diego, CA, USA.

Tuesday: 14:00-15:40
TC3: SYSTEM AND DEVICE MODELING
Chair: **G. Robins**, University of Virginia, Charlottesville, VA, USA.

14:00
TC3.1
SOC MODELING METHODOLOGY FOR ARCHITECTURAL EXPLORATION AND SOFTWARE DEVELOPMENT, M. Silbermintz, A. Sahar, I. Peled, M. Anschel, E. Watralov, H. Miller, E. Weisberger, Motorola Semiconductor Israel, Herzelia, Israel.

14:20
TC3.2
ENHANCEMENT OF THE SEMISYMBOLIC ANALYSIS PRECISION USING THE VARIABLE-LENGTH ARITHMETIC, J. Dobes, J. Michal, Czech Technical University, Praha, Czech Republic.

14:40
TC3.3
MODELING OF ANALOG CIRCUITS BY USING SUPPORT VECTOR REGRESSION MACHINES, A. Baric, V. Ceperic, University of Zagreb, Zagreb, Croatia.

15:00
TC3.4
ANALYSIS OF HARMONIC DISTORTION IN DEEP SUBMICRON CMOS, M. Bucher, A. Bazigos, N. Nastos, Y. Papananos, F. Krummenacher, S. Yoshitomi, Technical University of Crete, Chania, Crete.

15:20
TC3.5
A COMPACT METHOD FOR OBTAINING THE HYPRID PARAMETERS OF THE BJT AMPLIFIER, A. M. Al-Smadi, Q. Al-Zobi, Yarmouk University, Irbid, Jordan.

Tuesday: 16:00-17:40
TC4: INTERCONNECT DESIGN
Chair**: A. Baric**, University of Zagreb, Croatia **/ A. Kolodny**, Technion, Haifa, Israel.

16:00
TC4.1
DESIGN AND MODELLING OF NETWORK ON CHIP INTERCONNECTS USING TRANSMISSION LINES, *A. Barger, *D. Goren, **A. Kolodny, *IBM, Haifa, Israel, **Technion, Haifa, Israel.

16:20
TC4.2
SIGNAL PROPAGATION WITHOUT DISTORTION IN DISPERSIVE LOSSY MEDIA, R. H. Flake, J. Biskup, The University of Texas at Austin, Austin, TX, USA.

16:40
TC4.3
OPTIMAL RESIZING OF BUS WIRES IN LAYOUT MIGRATION, *S. Wimer, **A. Kolodny, **S. Michaely, *Intel, Haifa, Israel, **Technion, Haifa, Israel.

17:00
TC4.4
BUFFER SIZING FOR DELAY UNCERTAINTY INDUCED BY PROCESS VARIATIONS, *D. Velenis, *R. Sundaresha, **E. G. Friedman, *Illinois Institute of Technology, Chicago, IL, USA, **University of Rochester, Rochester, NY, USA.

17:20
TC4.5
OPTIMIZATION OF CHIP LEVEL CLOCK TREE PERFORMANCE BY USING
SIMULTANEOUS DRIVERS AND WIRE SIZING, S. Greenberg, I. Bloch, A. Maman, M. Horowitz, Motorola Semiconductor Israel, Omer, Israel, Ben-Gurion University, Beer-Sheva, Israel.

Hall: Arbel

Tuesday: 9:00 – 10:40
TA1.4
GRAND CHALLENGES IN SPATIAL-TEMPORAL COMPUTING ON IMAGE FLOWS, T. Roska, Hungarian Academy of Sciences and the Pazmany P. Catholic University, Budapest, Hungary

Tuesday: 11:00-12:40
TD2: BIOMEDICAL AND INDUSTRIAL APPLICATIONS
Chair: **R. Ginosar,** VLSI Systems Research Center, Technion, Haifa, Israel/ **A. Morgenshtein,** Technion, Haifa, Israel

11:00
TD2.1
NEW ISFET CATHETERS ENCAPSULATION TECHNIQUES FOR BRAIN PH IN-VIVO MONITORING, L. Sudakov-Boreysha, U. Dinnar, Y. Nemirovsky, Technion, Haifa, Israel.

11:25
TD2.2
THE ESO- PILL™ TM A NON-INVASIVE MEMS CAPSULE FOR BOLUS TRANSIT MONITORING IN THE ESOPHAGUS, *Y. T. Jui, **D. Sadowski, *K. Kaler, *M. Mintchev, *University of Calgary, Calgary, Alberta, Canada, **University of Alberta, Edmonton, Alberta, Canada.

11:50
TD2.3
MICROLENS ARRAY HELP IMAGING HIDDEN OBJECTS FOR MEDICAL APPLICATIONS, D. Abookasis, J. Rosen, Ben-Gurion University, Beer-Sheva, Israel

12:15
TD2.4
IMPROVEMENT OF ILLUMINATION ARTIFACTS IN MEDICAL ULTRASOUND IMAGES USING A BIOLOGICALLY BASED ALGORITHM FOR COMPARISON OF WIDE DYNAMIC RANGE, H. Spitzer, Y. Zimmer, Tel-Aviv University, Tel-Aviv, Israel.

Tuesday: 14:00-15:40
TD3: CONTROL SYSTEMS AND APPLICATIONS
Chair: **Y. Bar-Shlomo**, Ort B. A. College of Engineering, Carmiel, Israel.

14:00
TD3.1
DISTRIBUTED SYSTEM DESIGN AND CONTROL VIA MULTIPLE OBJECTIVES OPTIMIZATION, *I. Rusnak, **A. Guez, **R. Cochran, *Rafael, Haifa, Israel, **Drexel University, Philadelphia, PA, USA.

14:20
TD3.2
CONTROLLING AN ELECTRICAL MOTION SYSTEM BY A LOAD INSTRUCTION DECODING ALGORITHM USING FPGA, A. Kuperman, S. Cooper, R. Rabinovici, Ben-Gurion University, Beer-Sheva, Israel.

14:40
TD3.3
NANOROBOTIC CHALLENGES IN BIOMEDICAL APPLICATIONS, DESIGN AND CONTROL, *A. Cavalcanti, ,*L.C. Kretly **L. Rosen, **M. Rosenfeld, **S. Einav, *Unicamp University of Campinas, Campinas, Brazil, **Tel Aviv University, Tel Aviv, Israel.

15:00
TD3.4
NUMERICAL ALGORITHM FOR MEASUREMENT OF ANGLE PHASE SHIFT FOR SINES SIGNAL, A. Aksamovic, S. Konjicija, University of Sarajevo, Sarajevo, Bosnia and Herzegowina**.**

15:20
TD3.5
A NEW METHOD TO ANALYSE THE UNIQUE STEADY STATE OF NONLINEAR NONAUTONOMOUS CIRCUITS, *,**F. Ping, **W. Erzhi, ***P. Cooke, *S. Yuanchun, *Logistical Engineering University, Chongqing, China, **Shenyang Polytechnic University, Shenyang, China, ***Adelaide University, North Terrace , South Australia.

Tuesday: 16:00-17:40
TD4: MICRO-OPTO-ELECTRO-MECHANICAL SYSTEMS
Chair: **J. G. Harris,** University of Florida, Gainesville, FL, U.S.A **/ R. Shavit**, Ben-Gurion University, Beer-Sheva, Israel

16:00
TD4.1
2D PHOTONIC CRYSTALS DEPOSITED ON POLYMER PIEZOELECTRIC SUBSTRATES - NEW KIND OF MOEMS, E. Bormashenko, R. Pogreb, O. Stanevsky, Y. Biton, Y. Bormashenko, V. Streltsov, Y. Socol, The College of Judea and Samaria, Ariel, Israel.

16:20
TD4.2
A METHOD TO DESIGN DWDM FILTERS ON PHOTONIC CRYSTALS, A. Perri, A. Giorgio, R. Diana, Polytechnic of Bari, Bari, Italy.

16:40
TD4.3
A NOVEL DESIGN AND FABRICATION METHOD OF SCANNING MICRO-MIRROR FOR RETINAL SCAN DISPLAYS, O. Cohen, Y. Nemirovsky, Technion, Haifa, Israel**.**

17:00
TD4.4
A NOVEL DESIGN AND FABRICATION METHOD OF A PYRAMIDAL SHAPE CHIP FOR SCANNING MICRO MIRROR, O. Cohen, A. Shai, Y. Nemirovsky, Technion, Haifa, Israel.

17:20
TD4.5
COMPACT RF-PHOTONIC CONFIGURATION FOR HIGHLY RESOLVED AND ULTRAFAST EXTRACTION OF CARRIER AND INFORMATION OF RADAR SIGNAL, *Z. Zalevsky, **A. Shemer, ***V. Eckhouse, ***D. Mendlovic, **** S. Zach *Bar-Ilan University, Ramat-Gan, Israel, **Tel-Aviv University, Tel-Aviv, Israel, ***Civcom Devices and Systems Inc., Petah-Tikva, Israel, **** Walles.

Hall:Yarden

19:45 – 22:30
Banquet

Wednesday, December 15

"Arbel & Tabor" Hall

Plenary session
8:00 – 8:55

Nanometer Era: 90-nm/65-nm Design Technologies and Beyond

Peter (Chung-Yu) Wu, National Chiao Tung University

Hall: Galil

Wednesday: 9:00 – 10:40
WA1: SOC DESIGN AND INTEGRATION
Chair **Y. Betser**, Saifun, Netanya, Israel.

9:00
WA1.1
AUTOMATIC HARDWARE-EFFICIENT SOC INTEGRATION BY QOS NETWORK ON CHIP, E. Bolotin, A. Morgenshtein, I. Cidon, R. Ginosar, A. Kolodny, Technion, Haifa, Israel.

9:25
WA1.2
MICRO-MODEM RELIABILITY SOLUTION FOR NOC COMMUNICATIONS, A. Morgenshtein, E. Bolotin, I. Cidon, A. Kolodny, R. Ginosar, Technion, Haifa, Israel.

9:50
WA1.3
PRACTICAL PERFORMANCE OF PLANAR SPIRAL INDUCTORS, A. Telli, METU, Ankara, Turkey.

10:15
WA1.4
CRITERION OF DESIGN FOR SMALL VALUE INTEGRATED SELF-INDUCTORS, * '**G. Petit, *R. Kielbasa, **V. Petit, *Supelec, Gif sur Yvette, France, **Thales Airborne Systems, Elancourt, France.

Wednesday: 11:00 – 12:40
WA2: HIGH PERFORMANCE ARCHITECTURES
Chair: **M. Werner**, Technion, Haifa, Israel

11:00
WA2.1
A HIGH PERFORMANCE DATA-PATH TO ACCELERATE DSP KERNELS, M. Galanis, C. Goutis, University of Patras , Patras, Greece.

11:25
WA2.2
A 64-WAY VLIW/SIMD FPGA PROCESSING ARCHITECTURE AND DESIGN FLOW, A. K. Jones, R. Hoare, I. Kourtev, J. Fazekas, D. Kusic, J. Foster, S. Boddie, A. Muaydh, University of Pittsburgh, Pittsburgh, PA, USA.

11:50
WA2.3
THE 1:10 PHASED DEMULTIPLEXER CIRCUIT, S. Poriazis, Phasetronic Laboratories, Athens, Greece.

12:15
WA2.4
SYSTEMC OPPORTUNITIES IN CHIP DESIGN FLOW, I. Yarom, G. Glasser, Intel, Jerusalem, Israel.

Wednesday: 14:00-15:40
WA3: ADVANCED SYNTHESIS AND VERIFICATION METHODOLOGIES
Chair: **I. Yarom**, Intel Corporation, Israel

14:00
WA3.1
TECHNIQUES FOR FORMAL TRANSFORMATIONS OF BINARY DECISION DIAGRAMS, [*]G. Kolotov, [**]I. Levin, [**]V. Ostrovsky, [*]Tel-Aviv University, Tel-Aviv, Israel, [**]Bar-Ilan University, Ramat-Gan, Israel

14:25
WA3.2
EVALUATING AND COMPARING SIMULATION VERIFICATION VS. FORMAL VERIFICATION APPROACH ON BLOCK LEVEL DESIGN, [*]E. Segev, [*]S. Goldshlager, [*]H. Miller, [*]O. Shua, [*]O. Sher, [**]S. Greenberg, [*]Motorola Semiconductor Israel, Omer, Israel, [**]Ben-Gurion University, Beer-Sheva, Israel

14:50
WA3.3
PATTERN SEARCH IN HIERARCHICAL HIGH LEVEL DESIGNS, [*]Z. Terem, [*]G. Kamhi, [**]M. Y. Vardi, A. Irron, [*]Intel, Haifa, Israel, [**]Rice University, Houston, TX, USA

15:15
WA3.4
META-HEURISTICS HYBRIDIZING INDEPENDENT COMPONENT ANALYSIS WITH GENETIC ALGORITHMS, J. Gorriz, C. G. Puntonet, E. Lang, M. Salmeron, University of Cadiz, Algeciras, Spain.

Hall Carmel

Wednesday: 9:00 – 10:40
WB1: IMAGE AND VISION SYSTEMS
Chair: **S. Greenberg**, Freescale Semiconductor, Israel **/ N. Intrator**, Tel-Aviv university, Tel-Aviv, Israel

9:00
WB1.1
IMAGE REGISTRATION AND MOSAICING OF NOISY ACOUSTIC CAMERA IMAGES, K. Kim, N. Intrator, N. Neretti, Brown University, Providence, RI, USA

9:20
WB1.2
DESIGN OF LOW CROSS-TALK IMAGE TRANSCEIVER DEVICE AND CONTROLLER CIRCUITRY, [*]U. Efron, [**]Y. David, [**]I. Baal-Zedaka, [**]N. Thirer, [*]Ben-Gurion University, Beer-Sheva, Israel, [**]Holon Academic Institute of Technology, Holon, Israel

9:40
WB1.3
ISFET CMOS COMPATIBLE DESIGN AND ENCAPSULATION CHALLENGES, L. Sudakov-Boreysha, A. Morgenshtein, U. Dinnar, Y. Nemirovsky, Technion, Haifa, Israel

10:00
WB1.4
COMPUTER AIDED DESIGN USING CGH OF A THREE-DIMENSIONAL OBJECTS, D. Abookasis, J. Rosen, Ben-Gurion University, Beer-Sheva, Israel

10:20
WB1.5
VLSI SENSOR FOR MULTIPLE TARGETS DETECTION AND TRACKING, *A. Fish, *A. Spivakovsky, *A. Goldberg, *, **O. Yadid-Pecht, Ben-Gurion University, Beer-Sheva, Israel, University of Calgary, Alberta, Canada.

Wednesday: 11:00 – 12:40
WB2: DIGITAL SIGNAL PROCESSING
Chair: **R. J. Chen**, National United University, Miao City, Taiwan **/ H. Aharoni**, Ben-Gurion University of the Negev, Israel.

11:00
WB2.1
HIGH SPEED ASSEMBLY FFT IMPLEMENTATION FOR MEMORY ACCSS REDUCTION ON DSP PROCESSORS, *Y. Tang, *Y. Wang, **J. G. Chung, **S. Song, **M. Lim, *University of Texas at Dallas, Richardson, TX, USA, **Chonbuk National University, Chonju, South Korea

11:20
WB2.2
VITERBI DETECTION ANALYSIS ON RLL SEQUENCES, P. M. Putinica, S. Stancescu, University Politehnica Bucharest, Bucharest, Romania

11:40
WB2.3
RECONSTRUCTION OF NONUNIFORMLY SAMPLED PERIODIC SIGNALS: ALGORITHMS AND STABILITY ANALYSES, E. Margolis, Y. C. Eldar, Technion, Haifa, Israel

12:00
WB2.4
MINIMAX SAMPLING WITH ARBITRARY SPACES, T. Dvorkind, Y. C. Eldar, Technion, Haifa, Israel

12:20
WB2.5
A STATISTICAL TECHNIQUE FOR THE DETERMINATION OF THE NOISE POWER GAIN IN HIGHER-ORDER SIGMA-DELTA A/D CONVERTERS EXCITED BY DC INPUT SIGNALS, B. Nowrouzian, N. A. Fraser, University of Alberta, Edmonton, Alberta, Canada.

Wednesday: 14:00-15:40
WB3: VLSI CRYPTOLOGY
Chair: **M. Ahmadi**, University of Windsor, Canada.

14:00
WB3.1
EFFICIENT IMPLEMENTATION OF THE KEYED-HASH MESSAGE AUTHENTICATION CODE (HMAC) USING THE SHA-1 HASH FUNCTION, A. Kakarountas, H. Mihail, A. Milidonis, C. Goutis, University of Patras, Patras, Greece.

14:25
WB3.2
COMPARISON OF THE HARDWARE ARCHITECTURES AND FPGA IMPLEMENTATIONS OF STREAM CIPHERS, M. Galanis, P. Kitsos, G. Kostopoulos, N. Sklavos, O. Koufopavlou, C. Goutis, University of Patras, Patras, Greece.

14:50
WB3.3
HIGH PERFORMANCE CRYPTOGRAPHIC ENGINE PANAMA: HARDWARE IMPLEMENTATION, G. Selimis, P. Kitsos, O. Koufopavlou, University of Patras, Patras, Greece.

15:15
WB3.4
BULK ENCRYPTION CRYPTO-PROCESSOR FOR SMART CARDS: DESIGN AND IMPLEMENTATION, N. G. Sklavos, G. Selimis, O. Koufopavlou, University of Patras, Patras, Achaia, Greece.

Hall Tabor

Wednesday: 9:00 – 10:40
WC1: DESIGN FOR TESTABILITY AND RELIABILITY
Chair: **Y. Rosenwaks**,. , Tel-Aviv University, Tel-Aviv, Israel

9:00
WC1.1
FAST HIGH-LEVEL FAULT SIMULATOR, K. Sapiecha, S. Deniziak, Cracow University of Technology, Cracow, Poland.

9:25
WC1.2
AUTOMATIC SYSTEM FOR VLSI ON-CHIP CLOCK SYNTHESIZERS CHARACTERIZATION, Y. Fefer, S. Sofer, Motorola Semiconductor Israel Ltd., Herzeliya, Israel.

9:50
WC1.3
INVESTIGATION OF ON-CHIP PLL IRREGULARITIES UNDER STRESS CONDITIONS CASE STUDY, Y. Fefer, Y. Weizman, S. Sofer, E. Baruch, Motorola Semiconductor Israel Ltd., Hertzliya, Israel.

10:15
WC1.4
ON-CHIP AREA-EFFICIENT SPECTRUM ANALYZER FOR TESTING ANALOG IC, *M. A. *Dominguez, *J. L. Ausin, **G. Torelli, *J. F. Duque-Carrillo, *University of Extremadura, Badajoz, Spain, ** University of Pavia, Pavia, Italy.

Wednesday: 11:00 – 12:40
WC2: SEQUENTIAL SYNTHESIS METHODOLOGIES
Chair: **D. Lubzens**, Technion, Haifa, Israel.

11:00
WC2.1
LURU: TIME-OPTIMIZED FPGA TECHNOLOGY MAPPING WITH CONTENT ADDRESSABLE MEMORIES, A. K. Jones, J. Lucas, R. Hoare, I. Kourtev, University of Pittsburgh, Pittsburgh, PA, USA.

11:25
WC2.2
ADVANCED TIMING OF LEVEL-SENSITIVE SEQUENTIAL CIRCUITS, B. Taskin, I. Kourtev, University of Pittsburgh, Pittsburgh, PA, USA.

11:50
WC2.3
PERFORMANCE IMPROVEMENT OF EDGE-TRIGGERED SEQUENTIAL CIRCUITS, B. Taskin, I. Kourtev, University of Pittsburgh, Pittsburgh, PA, USA.

12:15
WC2.4
DESIGN OF DOUBLY COMPLEMENTARY FILTER PAIRS WITH CANONICAL SIGNEDDIGIT COEFFICIENTS USING GENETIC ALGORITHM, L. Liang, M. Sid-Ahmadi, University of Windsor, Windsor, Canada**.**

Wednesday: 14:00-15:40
WC3: LOW NOISE AMPLIFIERS
Chair: **I. Filanovsky**, University of Alberta, Canada

14:00
WC3.1
A DESIGN FLOW FOR INDUCTIVELY DEGENERATED LNA'S, D. Guermandi, E. Franchi, A. Gnudi, University of Bologna, Bologna, Italy.

14:25
WC3.2
DESENSITIZED DESIGN OF MOS LOW NOISE AMPLIFIERS BY R_n MINIMIZATION, *G. Banerjee, *D. Becher, *C. Hung, *K. Soumyanath, **D. Allstot, *Intel Corporation, Hillsboro, OR, USA, **University of Washington, Seattle, WA, USA.

14:50
WC3.3
A HIGH-SPEED CMOS OP-AMP DESIGN TECHNIQUE USING NEGATIVE MILLER CAPACITANCE, B. Shem-Tov, M. Kozak, E. G. Friedman, University of Rochester, Rochester, NY, USA.

15:15
WC3.4
ADAPTIVE ANALOG-TO-DIGITAL CONVERSION USING SELF-DITHERING IN DATA ACQUISITION SYSTEMS, *,**J. M. D. Dias Pereira, *P. S. Girao, **O. Postolache, Instituto de Telecomunicacoes, Lisbon, Portugal, **Escola Superior de Tecnologia, Setubal, Portugal.

Hall Arbel

Wednesday: 9:00 – 10:40
WD1: SPECIAL SESSION - RE-INVENTING METHODS AND TOOLS FOR NEXT-GENERATION CMOS DESIGN
Chair: **H. Yeshurun**, TAU, Tel Aviv, Israel.

9:00
WD1.1
PERSPECTIVES ON SCALING THEORY AND CMOS TECHNOLOGY: UNDERSTANDING THE PAST, PRESENT, AND FUTURE, PART I, D. Foty, Gilgamesh Associates, Fletcher, VT, USA.

9:20
WD1.2
PERSPECTIVES ON SCALING THEORY AND CMOS TECHNOLOGY: UNDERSTANDING THE PAST, PRESENT, AND FUTURE, PART II, D. Foty, Gilgamesh Associates, Fletcher, VT, USA.

9:40
WD1.3
ADVANCED COMPACT MODELS: GATEWAY TO MODERN CMOS DESIGN, PART I, *G. Gildenblat, **C. McAndrew, *H. Wang, *W. Wu, ***D. Foty, ****L. Lemaitre, *****P. Bendix, *The Pennsylvania State University, University Park, PA, USA, **Motorola Inc., Tempe, AZ, USA, ***Gilgamesh Associates, Fletcher, VT, USA, ****Motorola Inc., Geneva, Switzerland, *****LSI Logic Corporation, Milpitas, CA, USA.

10:00
WD1.4
ADVANCED COMPACT MODELS: GATEWAY TO MODERN CMOS DESIGN, PART II, *G. Gildenblat, **C. McAndrew, *H. Wang, *W. Wu, ***D. Foty, ****L. Lemaitre, *****P. Bendix, *The Pennsylvania State University, University Park, PA, USA, **Motorola Inc., Tempe, AZ, USA, ***Gilgamesh Associates, Fletcher, VT, USA, ****Motorola Inc., Geneva, Switzerland, *****LSI Logic Corporation, Milpitas, CA, USA.

10:20
WD1.5
PRACTICAL ASPECTS OF MOS TRANSISTOR MODEL "ACCURACY" IN MODERN CMOS TECHNOLOGY, *P. Bendix, **D. Foty, *D. Pachura, *LSI Logic Corporation, Milpitas, CA, USA, ** Gilgamesh Associates, Fletcher, VT, USA.

Wednesday: 11:00 – 12:40
WD2: IMAGE PROCESSING
Chair **A. Morgenshtein**, Technion, Haifa, Israel

11:00
WD2.1
A ROBUST AND FAST MODEL-BASED ATHLETE CONTOUR TRACKING IN DIVING VIDEOS, Y. Xiong, Y. Zhang, D. Yao, Tsinghua University, Beijing, China.

11:25
WD2.2
EFFICIENT GABOR EXPANSION USING NON MINIMAL DUAL GABOR WINDOWS, Nagesh K. Subbanna, Yonina Eldar, Technion, Haifa, Israel.

11:50
WD2.3
EFFICIENT LDPC CODES FOR JOINT SOURCE-CHANNEL CODING, H. Kfir, I. Kanter, Bar- Ilan University, Ramat-Gan, Israel.

12:15
WD2.4
ULTRA LOW-POWER DFF BASED SHIFT REGISTERS DESIGN FOR CMOS IMAGE SENSORS APPLICATIONS, *A. Fish, *V. Mosheyev, *V. Linkovsky, *,**Orly Yadid-Pecht, *Ben-Gurion University, Beer-Sheva, Israel, **University of Calgary, Alberta, Canada.