

ICECS 2004

The 11th IEEE International Conference on Electronics,
Circuits and Systems.

December 13 – 15, 2004

Tel Aviv, Israel

**Conference Guide
&
Abstract Book**

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Tel Aviv, 2004

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General Chair's Welcome Message

Dear Colleagues working in the Circuits and Systems field – welcome to Israel!

This is the 11th IEEE International Conference on Electronics, Circuits and Systems, held for the first time in Tel-Aviv. ICECS has started out in the warm climate of the Middle East (Egypt), and is continuing in Tel-Aviv as an IEEE-CAS venue providing a welcome respite from the cold European winter along the balmy Mediterranean shores.

Thanks to the efforts of many around the world, we are able to offer a rich, high quality technical program spread over three days. We have invited three plenary keynote speakers, two from the academia and one from the industry. The keynote topics will provide a fascinating overview of circuits and systems in different fields. In addition, several special sessions have been organized on topics that have recently attracted attention, ranging from nano-scale technology to grand challenges in different circuits and systems fields. Also on the agenda are 6 half-day tutorials covering a wide range of topics: Operational Amplifiers, Analog Circuit Design Methodology, Video Processing, CMOS Imagers, the MOS Transistor, Computer Vision, and SOI CMOS.

The organization of an international conference is a major effort and requires the input, creativity and energy of many people. My thanks go to the Technical Program Committee Chair and members, to our conference manager and the people at the VLSI Systems Center at the Ben-Gurion University, who worked on the tasks at hand on a daily basis and learned a great deal about all the issues involved in organizing such international venue.

Our conference manager has arranged a very attractive social program that starts with a welcome reception on Sunday evening. You will get a taste of Tel-Aviv's history on Monday evening during the visit to the "white city" - as Tel Aviv was proclaimed by UNESCO in its list of world cultural heritage sites. On Tuesday evening the banquet dinner will take place with special guests of honor. In addition, you are invited to join us every evening for the Hanukah Candles lighting – a Jewish tradition performed during the Hanukah Holiday, the "Holiday of Lights", which takes place these days.

The IEEE Circuits and Systems Society provided overall sponsorship for the conference, and I thank them for their support. Additionally, I would like to thank our industrial partners: Freescale Semiconductors, Tower Semiconductor Ltd., IBM Israel, Orbotech and Intel Israel, for their generous sponsorship of this event.

We can certainly say that this conference offers a unique forum for researchers and practitioners from academia, industry and government to share their expertise, results, and achievements in all areas of circuits and systems.

Many individuals have contributed to the success of this conference. My sincere thanks go to all authors including those whose papers were not

included in the program. Many thanks go to the Technical Program Committee members and the reviewers, and to the Steering Committee members, who sacrificed their time to make this event a first-class conference. Special thanks go to Professor Eby Friedman, our Technical Program Chair, for his tireless work in finalizing this outstanding technical program. Thanks are due to Professor George Moschytz for his ongoing support throughout the different stages. My thanks go also to our conference secretary, Professor Aryeh Weiss and to our treasurer, Professor Yisroel Rotman for their help, and to Professor John Harris and Professor Peter Wu for their enthusiasm and energy driving the special sessions.

I would also like to especially acknowledge our conference manager, Tami Polna-Guata who put much effort in making this conference a big success, and to Rachel Mahluf-Zilberberg, Vered Nitzan and Ruslan Sergienko for their continuous work on it.

Last but not least, I would like to thank my loved ones who put up with me all this time...

Enjoy the conference!

Orly Yadid-Pecht
General chair, ICECS 2004

A Message from the Technical Chair

On behalf of the technical program committee of this year's IEEE International Conference on Electronics, Circuits and Systems, I am delighted to welcome everyone to Israel. This year's ICECS conference is particularly exciting, both technically and culturally, and having Israeli participation in the ICECS conference is important to both Israel and ICECS.

The conference includes traditional concentration areas in analog and digital microelectronics circuits and systems along with more exotic topics such as VLSI cryptology, micro-opto-electro-mechanical systems, and biomedical and industrial applications. There is much for everyone. I should like to note that the quality of the papers is particularly high, and I am confident that the conference attendees will enjoy the technical program. For example, we have four exciting special sessions on microelectronics technologies included in the program, such as nanoelectronics, nanotechnology, and giga-scale systems, grand challenges in circuits and systems, re-inventing methods and tools for next generation CMOS design, and neuromorphic systems.

We have a very strong program composed of 36 sessions and 168 papers over three days. Authors from around the world will be attending and presenting their research results. Papers originating from the United States, China, India, Jordan, Spain, Italy, Japan, Brazil, Greece, Romania, Mexico and, of course, Israel, will be presented.

A total of 212 papers were submitted, from which 168 high quality papers were accepted (79%). A total of 752 reviews were received from all over the world, permitting an average of three to four independent reviews per paper.

I am also thrilled to mention that we have three outstanding keynote presentations from world-wide experts in the fields of electronics, circuits, and systems. These experts and their talks are Prof. George Moschytz on "From LC filters to filters-on a-chip: a technological odyssey," Dr. Uri Weiser on "Microprocessors: bypass the power wall," and Prof. Chung-Yu Wu on "Nanometer era: 90-nm/65-nm design technologies and beyond."

In addition to the technical program, we will have a large variety of social activities. We are also fortunate that the conference is at the same time as Hanukah, our Jewish holiday of light and redemption. I am confident that all will enjoy the energy and traditions that are everywhere within Israel and at our annual ICECS.

I would like to express my sincere appreciation to Prof. Orly Yadid-Pecht for her enthusiastic and focused effort in making this conference a success. Without her involvement, this conference would simply not have occurred, as well as having such an outstanding technical and social program. I would also like to thank Tom Wehner for his web-based review system and for all of the support he provided throughout the paper review and proceedings development process and Prof. John Harris for his help with the special sessions.

Finally, I would like to thank Jonathan Rosenfeld for making the technical program happen. He did all of the real work, and did an absolutely outstanding job. Thank you Yoni.

Thank you all very much for coming. I am sure you will have a great time.

Eby G. Friedman
ICECS 2004 Technical Chair

Conference Organization

Co-Organized by:

Ben-Gurion University of the Negev, Beer-Sheva, Israel
The VLSI Systems Center, Ben-Gurion University of the Negev, Beer-Sheva, Israel.

Sponsored by:

IEEE Organization

IEEE Circuits and Systems Society

Freescale Semiconductor Inc.

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Organizing Committee

General Chair

Orly Yadid-Pecht,
The VLSI Systems Center, Ben-Gurion University, Beer-Sheva, Israel
Department of Electrical Engineering, University of Calgary, Alberta,
Canada.

Technical Program Chair

Eby Friedman,
University of Rochester, Rochester, NY, USA.

Plenary Sessions Chair

George Moschytz,
Swiss Federal Institute of Technology and Bar-Ilan University, Israel.

Local Arrangements Chair

Yosi Shacham-Diamand,
Tel-Aviv University, Israel.

Finance Chair

Stanley Rotman,
Ben-Gurion University, Israel.

Proceedings Chair

Anthony J. Weiss,
Tel-Aviv University, Israel.

Publicity Chair

Yacov Malinovich,
ColorChip Ltd., Israel.

Ilan Rusnak,
Rafael, Israel.

Special Sessions Chair

John Harris,
University of Florida, FL, USA.

Tutorials Chair

Andreas Andreou,
Johns Hopkins University, Baltimore, MD, USA.

Registration Chair

Uzi Efron,
Ben-Gurion University, Israel.

Secretary

Aryeh Weiss,
Bar-Ilan University, Ramat-Gan, Israel.

Steering Committee Members (ICECS 2004)

Adrijan Baric, University of Zagreb, Croatia
Magdy Bayoumi, University of Louisiana at Lafayette, USA
John Choma, University of Southern California, USA
Malgorzata Chrzanowska-Jeske, Portland State University, USA
Ayman Ibrahim El Dessouki, Electronic Research Institute, Egypt
Jose Franca, Instituto Superior Tecnico, Portugal
Eby Friedman, University of Rochester, USA
Mohammed Ismail, Ohio State University, USA
Odysseas Koufopavlou, University of Patras, Greece
Tor S. Lande, University of Oslo
Piero Malcovati, University of Pavia, Italy
Franco Maloberti, Texas A&M University, USA
Joseph Micallef, University of Malta, Malta
George Moschytz, ETH Zurich, Switzerland
Mohammad S. Obaidat, Monmouth University, USA
Branimir Pejcinovic, Portland State University, USA
Veikko Porra, Helsinki University of Technology, Finland
Mohamad Sawan, Ecole Polytechnique de Montreal, Canada
Abdallah Sfeir, Lebanese American University, Lebanon
Dimitrios Soudris, Democritus University of Thrace, Greece
Thanos Stouraitis, University of Patras, Greece
Hannu Tenhunen, Royal Institute of Technology, Sweden
Orly Yadid-Pecht, Ben-Gurion University, Israel
Al-Mualla , Etisalat College, U.A.E.
Bassel Soudan, University of Sharjah, U.A.E.

Technical Program Committee

Prof. Eby Friedman, Israel (Chair)
Prof. Orly Yadid-Pecht, Israel
Prof. Peter Wu, Taiwan
Prof. Tor Sverre Lande, Norway
Prof. Adrijan Baric, Croatia
Prof. Yacov Bar-Shlomo, Israel
Prof. Majid M. Ahmadi, Canada
Prof. Thanos Stouraitis, Greece
Prof. Bill Cheng-Fang Tai, Taiwan
Prof. Rong-Jian Chen, Taiwan
Prof. Martin P. Mintchev, Canada
Prof. Brita Olson, USA
Prof. Ljiljana Trajkovic, Canada
Prof. Nahum Kiryati, Israel
Prof. Izzet Kale, UK
Prof. Dimitris Velenis, USA
Prof. Luigi Fortuna, Italy
Prof. Anthony Maeder, Australia
Prof. Malgorzata Chrzanowska-Jeske, USA
Prof. Peter Pirsch, Germany
Dr. David Levy, Israel
Dr. Magdy Bayoumi, USA
Dr. Michael Zelikson, Israel
Dr. Wouter A. Serdijn, Netherlands
Dr. Avinoam Kolodny, Israel
Dr. Bing Sheu, USA
Dr. Israel A. Wagner, Israel
Dr. Esther Rodriguez-Villegas, UK
Mr. Tiberiu Galambos, Israel

Session Chairs

Monday, December 13, 2004

C. F. Tai	ANALOG AMPLIFIERS	MA1
S. Engelberg	NONLINEAR CIRCUITS	MB1
A. Kolodny	INTERCONNECT MODELING	MC1
C. Y. Wu	SPECIAL SESSION: NANOELECTRONICS, NANOTECHNOLOGY, AND GIGA-SCALE SYSTEMS	MD1
I. Filanovsky	RF OSCILLATORS	MA2
A. I. Perez / D. Sadot	COMMUNICATION SYSTEMS	MB2
Y. Nemirovsky	CMOS IMAGING SENSORS	MC2
J. G. Harris	SPECIAL SESSION: NEUROMORPHIC SYSTEMS	MD2
G. S. Moschytz	ANALOG FILTERS	MA3
R. Holzer	SIGMA-DELTA MODULATORS	MB3
D. Allstot	HIGH PERFORMANCE INTEGRATED CIRCUITS	MC3
A. Baric / D. Foty	NEURAL NETWORKS	MD3

Tuesday, December 14, 2004

J. G. Harris	SPECIAL SESSION: GRAND CHALLENGES IN CIRCUITS AND SYSTEMS	TA1
T. Galambos	CONVERSION CIRCUITS	TA2
S. Greenberg	VIDEO AND MULTIMEDIA TECHNOLOGY	TB2
G. Robins	PROCESS AND DEVICE SIMULATION	TC2
R. Ginosar / A. Morgenshtein	BIOMEDICAL AND INDUSTRIAL APPLICATIONS	TD2
P. Schechner	POWER ELECTRONICS	TA3
I. Wagner / J. Shappir	MIXED-SIGNAL CIRCUITS	TB3
G. Robins	SYSTEM AND DEVICE MODELING	TC3
Y. Bar-Shlomo	CONTROL SYSTEMS AND APPLICATIONS	TD3
T. Galambos	ANALOG CIRCUITS AND APPLICATIONS	TA4
M. A. Lagunas	COMMUNICATION RECEIVERS	TB4
A. Baric / A. Kolodny	INTERCONNECT DESIGN	TC4
J. G. Harris / R. Shavit	MICRO-OPTO-ELECTRO-MECHANICAL SYSTEMS	TD4

Wednesday, December 15, 2004

Y. Betser	SOC DESIGN AND INTEGRATION	WA1
S. Greenberg /N. Intrator	IMAGE AND VISION SYSTEMS	WB1
Y. Rosenwaks	DESIGN FOR TESTABILITY AND RELIABILITY	WC1
H. Yeshurun	SPECIAL SESSION: RE-INVENTING METHODS AND TOOLS FOR NEXT-GENERATION CMOS DESIGN	WD1
M. Werner	HIGH PERFORMANCE ARCHITECTURES	WA2
R. J. Chen / H. Aharoni	DIGITAL SIGNAL PROCESSING	WB2
D. Lubzens	SEQUENTIAL SYNTHESIS METHODOLOGIES	WC2
A. Morgenshtein,	IMAGE PROCESSING	WD2
I. Yarom	ADVANCED SYNTHESIS AND VERIFICATION METHODOLOGIES	WA3
M. Ahmadi	VLSI CRYPTOLOGY	WB3
I. Filanovsky	LOW NOISE AMPLIFIERS AND ADAPTIVE PROCESSING	WC3

Reviewers List

Abbaspour	Soroush
Abed	Khalid
Aggarwal	Apoorv
Aghaghiri	Yazdan
Ahmadi	Majid
Akgun	Omer Can
Aktas	Adem
Al-Ginahi	Yasser
Al-Janabi	Mohammed
Alarcon	Eduard
Anderson	Betty Lise
Andreev	Boris
Au	Oscar
Bagga	Sumit
Bahar	Iris
Balakrishnan	Mahadevan
Bar-Shlomo	Yacov
Barnea	Ofer
Bartolic	Juraj
Bayoumi	Magdy
Bazes	Mel
Ben-Hanan	Uri
Benabes	Philippe
Berberidis	C
Bisdounis	Labros
Bogunovic	Nikola
bonomo	claudia
Bor	Jenn-Chyou
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Bruck	Yurri
Bubis	Eugenia
Bunch	Robert
Burdo	Gennady
Butkovic	Zeljko
Carmona	Ricardo
Cetin	Ediz
Chang	Chen-Hao

Chang	Joseph
Chang	LiFu
Chatriki	Harsha
Chaudhary	Kamal
Chen	Guanrong
Chen	Guoqing
Chen	Quentin
Chen	Rong-Jian
Cheng	Yi
Cho	Hyoung
Chrzanowska Jeske	Malgorzata
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Cintra	Renato
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Cong	Jason
Constandinou	Timothy
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Dalbelo-Basic	Bojana
Dallet	Dominique
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Darmanjian	Shalom
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Dehnhard	Andreas
Delbruck	Tobias
Dimitrov	V
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Dobes	Josef
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Economides	Anastasios
El-Feghi	Idris
El-Gamal	Mourad
El-Moursy	Magdy
Elgharabawy	Waleed
Erdogmusb	Deniz
Feely	Orla
Ferentinos	Vissarion
Filanovsky	Igor
Fischer	Godi
Fitzsimmons	Mike

Fleshel	Leonid
Foty	Daniel
Fox	Rob
Frasca	Mattia
Friebe	Lars
Galambos	Tiberiu
Galivanche	Rajesh
Gattiker	Giorgio
Ghosh	Soumik
Giaquinto	Nicola
Ginosar	Ran
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Hassibi	Babak
Helfenstein	Markus
Hernandez	Luis
Heydari	Payam
Hossam	Fahmy
Hou	Yu
Hsiung	Pao-Ann
Hu	Jiang
Huang	Hong-Yi
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Ismail	Yehea
J Chen	Kevin
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Jairath	Akash
Jakobson	Claudio
Jalali-Farahani	Bahar

Jeppson	Kjell
Kang	Changwoo
Kang	Sung Mo
Kapus	Tatjana
Kapus-Kolar	Monika
Karim	Karim
Ker	Ming Dou
Kim	Suki
Klausen	Ralf
Klemp	Oliver
Klussmann	Heiko
Knoll	Ernest
Koh	Cheng-Kok
Kolodny	Avinoam
Kotek	Daniel
Kozak	Muchit
Krukowski	Artur
Kukimoto	Yuji
Kursun	Volkan
Lach	John
Lagudu	Sateesh
Lai	Jui-Lin
Langemeyer	Stefan
Lavi	Yoav
Li	Xun
Li	Yuan
Lim	Su-Tarn
Lin	Chin-Teng
Linan	Gustavo
Liow	Yu-Yee
Liu	Shih-Chii
Lopez-Martin	Antonio
Luo	Qiang
Lutovac	Miroslav
Magen	Nir
Malcovati	Piero
Manabe	Takeshi
Masselos	Konstantinos
Mayaram	Kartikeya
McGrath	D.

Meolic	Robert
Minch	Bradley
Moch	Soeren
Moon	Un-Ku Moon
Moreinis	Michael
Morgenshtein	Arkadiy
Morris	Steve
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Narroschke	Matthias
Naskas	Nikos
Natarajan	Sreedhar
Ndjountche	Tertulien
Newcomb	Robert
Ng	Tung-sung
Ngarmnil	Jitkasame
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Pomeranz	Irith
Popovich	Mikhail
Poulin	Pierre
Prashant	Suryanarayan
Psychalinos	Costas
Qi	Xin
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Ramirez-Angulo	Jaime
Ramu	Karthick
Rankov	Aleksandra
Reimer	Klaus
Reiner	Thomas

Reuter	Carsten
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Rosenfeld	Jonathan
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Schmookler	Marty
Schneider	Marcio
Schwartz	Odelia
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Serdijn	Wouter
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Sheinman	Benny
Sherman	Anatoly
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Tsakalides	Panagiotis
Tse	Chi Kong
Urey	Hakan

Vallina	Fernando
van Hartingsveldt	Koen
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Vohra	Neeti
Vouzis	Panayiotis
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Wang	Jinn-Shyan
Wang	Zen-Chieh
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Weiser-Biton	Rivka
Weissenfeld	Axel
Werner	Michael
Wilton	Steve
Winter	Matthias
Yamazaki	Akira
Yang	Wei-Bin
Yen	Vincent
Yifrach	Y
Yue	Chi-Yao
Zare-Hoseini	Hashem
Zemva	A.
Zhang	Junmou
Zhang	Ling
Zygouris	Vaggelis

Conference Highlights

The ICECS 2004 Conference will take place from 13 -15 December 2004 at the Sheraton Moriah Hotel, Tel Aviv, Israel.

This year's ICECS conference is particularly exciting, both technically and culturally. The conference includes traditional concentration areas in analog and digital microelectronics circuits and systems along with more exotic topics such as VLSI cryptology, micro-opto-electro-mechanical systems, and biomedical and industrial applications. There is much for everyone.

A day previous to the conference two interesting Tutorials will take place. Throughout the conference we will have three outstanding keynote presentations from worldwide experts in the fields of electronics, circuits, and systems and four exciting special sessions on microelectronics technologies are included in the program, as well as many interesting sessions.

The best paper award will be presented at the closing ceremony, the Banquet Dinner on Wednesday, December 14 2004.

We also organized a very colorful and varied social program.

Tutorials (Half-day)

Morning Tutorial: Sunday December 12, 2004, 9:00-12:30

Hall: Carmel

Vadim V. Ivanov / I. M. Filanovsky - **Circuit Techniques for Operational Amplifier Speed and Accuracy Improvement: Analog Circuit Design with Structural Methodology.**

Afternoon Tutorial: Sunday December 12, 2004, 13:30-17:00

Hall: Carmel

Andreas G. Andreou - **Mixed Analog/Digital Circuits in SOI CMOS.**

Registration Desk

Hours: Saturday: 14:00 – 17:00

Sunday: 8:00 – 17:00

Monday: 8:00 – 18:30

Tuesday, Wednesday: 7:30 – 18:30

ICECS 2004 Secretariat e-mail: icecs2004@icecs2004.org

Message center

Message center will be situated at the Conference Registration Desk.

Internet center

Internet center access for e-mail will be available near the Registration Desk. It will consist of three internet computer positions and two connections to Laptops.

Preview Desk

Preview Desk is located at the Internet center and will be accessible during registration hours. Authors are requested to hand over their presentations, on CD or Disk on key in advance, in order to arrange their presentation automatically.

Proceeding CD-ROM

Conference registrants can purchase extra copies of the Proceeding CD-ROM at the Registration Desk.

Best paper award

All papers published in the proceedings and presented at the conference were eligible for the award. Initial screening of candidates was based on reviewer's scores. A special committee narrowed down the twelve finalists to six, then made the final decision.

The award will be presented at the closing ceremony, the Banquet Dinner on Wednesday, December 14 2004.

Services

We have arranged some services for your convenience: Those services should be purchase in advance.

Lunch coupons at special conference rate, for the hotel restaurant are available at the conference registration desk.

Parking vouchers, for "Kikar Atarim" parking lot can be purchased from the Bellboy desk, at the hotel entrance (25 NIS per day).

Tourist Information Desk

Tourist Information Desk will be operated next to the Conference Registration Desk.

Social Program

Welcome Reception

Sunday, Dec. 12, 20:00- 21:30, "Yarden" Hall, Sheraton Moriah Hotel.

An Evening Tour in Rothschild Boulevard:

Monday, Dec.13, 19:00 - 21:00

This tour includes stories about the buildings in the boulevard and the people who lived in them. We'll also find a bit of nostalgia from Little Tel Aviv, and will visit the Independence Hall, where the State of Israel was proclaimed, courtesy of the Association for Tourism of Tel Aviv-Jaffa.

Everyone is welcome to join free of charge.
Departure from Sheraton Moriah Hotel lobby.

Banquet Dinner:

Tuesday, Dec.14, 19:45 - 22:30, "Yarden" Hall, Sheraton Moriah Hotel.

Program of Optional Tours

ICECS 2004 organizers have arranged four interesting excursions that will best present the beauties of Israel:

Tour No. 1 Jerusalem of Gold

Date: 12 or 16 of December 2004

Fee: 65 \$

Full day tour: (08:00-18:00)

A viewpoint on the Mount of Olives, offers us a beautiful panorama of the whole city of Jerusalem.

Christian quarter: Holy Sepulcher (The Tomb of Jesus) and Via Dolorosa.

The Jewish quarter: A visit to the Western Wall ("Wailing Wall") and observation of the Dome of the Rock.

A visit to the Davidson Museum, exhibit a simulation of the period of second temple in Jerusalem and Western Wall Tunnels.

Tour No. 2 Massada National Park and the Dead Sea

Date: 12 of December 2004

Fee: 75 \$

Full day tour: (08:00-18:00)

Massada - a symbol of willpower and heroism. Sitting on an isolated cliff in the Judean Desert, Massada's steep slopes and precipices rise more than 1,300 feet (400 meters) above the Dead Sea. The combination of cliffs and escarpments in the desert area provided Massada with the perfect natural defense system, which tells us an heroic story...

The Dead Sea. The Dead Sea, the lowest point on earth and the largest "Natural Spa" in the world, is also one of the world's true natural wonders and a unique tourism destination. The Dead Sea is the saltiest and most mineral-laden body of water in the world. We will stop for a dip at the Dead Sea or smear of medicinal mud.

Tour No. 3 The Sorek Cave & Mini Israel

Date: 16 of December 2004

Fee: 65 \$

Half day tour: (08:00-15:00)

The Sorek Cave - The most beautiful Stalactite and Stalagmite Cave in Israel, with a variety of magnificent formations located on the slopes of the Judean Hills.

Mini Israel - See it all: Small Mini models of numerous well-known Israeli Sites. A most exciting attraction. It features over 350 exact replica hand crafted models of the holy land, telling the story of the people and the land of Israel.

Tour No. 4 The City of Caesarea and Haifa

Date: 16 of December 2004

Fee: 65 \$

Full day tour: (08:00-18:00)

The City of Caesarea. The well-known city of Caesarea was built by Herod the great. Herod constructed a deep-sea harbor and built storerooms, markets, wide roads, baths, temples, and luxurious public buildings. Every five years the city hosted major sports competitions, gladiator games, and theatrical productions.

The city of Haifa has a sweeping panoramic view. It is located on the slopes of Mount Carmel. We will visit the outdoor Exhibitions in the alleys of the *Wadi Nisnas neighborhood* - cultural and artistic expression of the good relations between Jews and Arabs living in peace and coexistence and experience the "Holiday of Holidays" festival (Hanuka, Ramadan and Christmas). We shall also visit the breath taking *Terraces of The Bahai Gardens*, the *German Colony* and the *Castra Art Center*.

Note! The tours will take place only if there are a minimum number of participants. The organizers reserve the right to cancel a given trip if the number of registrants is low, in which case the trip registration fees will be refunded in full.

About Israel

The State of Israel is located between the eastern shores of the Mediterranean Sea and the head of the Gulf of AQABA, an arm of the Red Sea. Israel was established on May 14, 1948, as a Jewish state. Israel is considered the Holy Land for Christians, Jews, and Muslims.

Tel Aviv-Jaffa

The city of Tel-Aviv is stretched along the beautiful beach strip of the Mediterranean; Tel-Aviv is Israel's largest city and biggest commercial center. It is a busy metropolis, which inspires its visitors with a unique energetic atmosphere of excitement and fun.

Visible from a distance with its seafront skyscrapers and exclusive hotels, Tel-Aviv presents a lively combination of entertainment venues, shopping

malls, exotic markets, nonstop active nightlife, gorgeous golden beaches and wonderful restaurants of all kinds.

It is also the country's greatest cultural center, a home for a variety of museums, galleries, theatres and concert halls. By contrast, the ancient port city of Jaffa, is medieval in appearance.

This special blend of Mediterranean ambience, seaside resort and modern facade is what makes the city so uniquely appealing. Tel Aviv and Israel are connected to the rest of the world via the international airport at Lod (BGA), 14 km (9 mi) southeast of the city; the port of Ashdod, 31 km (19 mi) to the south; and the port of Haifa, 80 km (50 mi) to the northeast.

"The White City" of Tel Aviv includes the world's largest grouping of buildings in the International Style, also known as Bauhaus. UNESCO, proclaimed it in July 2003, as a World Cultural Heritage site, in recognition of the special architectural qualities of the buildings, streets, squares and boulevards of the White City.

In the 1930's, many immigrants came to Tel Aviv from Germany, numbering among them, the young architects Arie Sharon and Yaakov Rechter, graduates of the Bauhaus School of Art and Design, who brought with them architectural styles and ideas, which were new for the period.

"The White City" is the story of Tel Aviv, from its beginning to the present time, and is a wonderful opportunity to savor the experience of life in Tel Aviv, in the past and in the present.

Security check

Security checks are carried out routinely for your protection and safety. We appreciate your understanding and patience.

At your departure from Israel, take in consideration that you have to be at the airport two and a half hours before your flight departure time, for security check and check in your flight.

El-Al offers an exclusive advance check-in service. For flights between 3am-4pm, check-in is the day before, Sunday through Thursday. Arlozorov Street Tel-Aviv (next to the Railway Station). The advanced check-in will save you time at the airport.

Climate

Israel enjoys long, warm, dry summers (April-October) and generally mild winters (November-March). Weather extremes range from occasional winter snowfall in the mountain regions to periodic oppressively hot dry winds that send temperatures soaring, particularly in the summer. Winters are mild, with temperatures averaging 14 degrees C (57 degrees F) along the coast and 9 degrees C (48 degrees F) in the mountains. The Dead

Sea area is the lowest place on the planet and the climate is one of the hottest regions in the world.

Language

The official languages of Israel are Hebrew and Arabic. English is widely used as a second language, and recently Russian has become commonplace.

People

The country is home to a diverse population from many ethnic, religious, cultural and social backgrounds. Of its more than 5.5 million population, 81.5 percent are Jews (over half are native born and mostly first and second generation), while the rest come from some 80 countries around the world; about 17% are Arabs (most of them are Moslem) and the remaining 1.5% are Christians, Druze, Circassian and other small communities.

Religion

Freedom of religion and the inviolability of the holy places and centers of worship for all religions are guaranteed by law.

The main religions in Israel are Judaism Islam and Christianity. There are many holly sights for all three religions spread all over the country, mainly in Jerusalem. Few of them are offered in our tours.

The Sabbath and Holidays

Israel's day of rest, the Sabbath (Saturday) and all Jewish holidays commence at sundown on the evening before the holiday and end the following night at sunset. Banks, businesses and public institutions are closed at these times. In the major cities, many restaurants, cinemas, nightclubs and discotheques remain open. The Hebrew calendar is based on the lunar year; therefore Jewish holidays fall on different Gregorian dates each year.

Hannukah - Festival of Lights

Sunday, December 8 is the first night of Hannukah - the Festival of Lights. Hannukah is an eight-day festival.

The Hannukah festival has accompanied the Jewish people from the time of the Greek occupation. Antiochus Epiphanes (164-175 B.C.E.), he exerted his authority over its political and social institutions, including that of the Temple of Jerusalem. The Jewish population was forbidden to exercise its religious precepts and ordered to carry out the Greek pagan

rites. This religious oppression finally culminated in an uprising, headed by the Maccabees, with the purpose of restoring religious and political freedom to the land.

Judah Maccabee led his forces, entered Jerusalem and the holy Temple. All they could find there was a small drop of oil in a little jug to light their lamp. The miracle that occurred, which forms the core of the Hannukah story, was that this drop of oil lasted for eight days and enabled the priests to purify the Temple and renew their holy rituals.

Israelis celebrate Hannukah traditionally throughout the country, with their families and friends, lighting the candles for eight nights, singing Hannukah songs and eating the traditional food of latkes (potato pancakes) and doughnuts. It is also the custom to give a gift to the children and for them to play with spinning tops. Hannukah is regarded by all as a wonderfully warm and joyful festival to celebrate. We wish you all a Happy Hannukah.

Passports and Visas

Every visitor to Israel must hold a valid passport; stateless persons require a valid travel document with a return visa to the country of issue. Visitors may remain in Israel for up to three months from the date of arrival, subject to the terms of the visa issued. Visitors who intend to work in Israel must apply to the Ministry of the Interior for a special visa (B/1).

Time difference

Israel is on the middle east time, which is about one hour different from European time, 7-10 hours from the USA and 4-7 hours from Asia.

Electricity

The electrical supply is 220 Volts, 50 Hertz. The two-pin plug system is used, like in the most of Europe.

Health

Travelers are not required certificates of vaccination or insulation to enter Israel. It is advisable to take out a personal medical insurance policy. Tap water is safe to drink.

The Tel-Aviv Medical Center –"Eichilov" hospital.

Weizmann 6 st. telephone- 03-6974444.

Ambulance services "Magen David Adom" In Case of EMERGENCY - Dial "101" .

Driving

The minimum driving age within Israel is 17. Driving is on the right side of the road.

The speed limit is 50 km/h in the city and 100 km/h on overland roads.

Table of distances between main cities

		kM	Miles
Tel Aviv	- Jerusalem	58	36
Tel Aviv	- Tiberias	134	83
Tel Aviv	- Haifa	95	59
Tel Aviv	- Beer sheva	105	65
Tel Aviv	- Eilat	346	120
Tel Aviv	- (Dead Sea)	184	115
Tel Aviv	- Rosh Hanikra	137	85

International Airport: Ben Gurion Airport - 19 Kilometers From Tel Aviv.

Currency

The basic Israeli currency is New Israeli shekel (NIS).

Foreign currency can be exchanged for local money in banks, post offices and exchange offices, according to the valid rates of exchange.

No commission is charged when exchanging foreign currency at American Express offices in Tel-Aviv and Jerusalem and at post office branches.

The Shekel

1 Shekel (N.I.S.) is 100 Agorot (ag.).

Bills:

200 Shekel - 200 N.I.S.

100 Shekel - 100 N.I.S.

50 Shekel - 50 N.I.S.

20 Shekel - 20 N.I.S.

Coins:

10 Shekel - 10 N.I.S.

5 Shekel - 5 N.I.S.

1 Shekel - 1 N.I.S.

50 Agorot - 0.50 N.I.S. - 50 ag.

10 Agorot - 0.10 N.I.S. - 10 ag.

Banks and ATM's

Most banks are normally open Sundays, Tuesdays and Thursdays from 8:30-9:00 till 12:30-13:00 and from 16:00-18:00; and on Monday, Wednesday and Friday during the morning hours only. There are ATM's located all over the city. Most international bankcards are accepted. Besides bank and exchange Bureau at the airport, you can exchange foreign currency at the exchange offices all over the city.

Credit cards

Most hotels and restaurants, as well as many shops accept AmEx, Master Card and Visa.

Telecommunication

Local and international calls can be made from the hotel. Call cards for public pay phone are available at every Post office. Israel (telephone) area code is 972-3 (Tel Aviv).

Transportation

International Airport: Ben Gurion Airport Information - 03-9755555.

Transit from Tel-Aviv Ben-Gurion airport is located approximately 20km from Tel-Aviv, about a 25-30 minute drive.

United Tours bus #222 runs from the cluster of Tel-Aviv hotels on Hayarkon St, to the youth hostel on Weizmann St and the Tel-Aviv train station on Arlozorof St to Ben-Gurion Airport departure hall.

Every 45 minutes, Sun-Thu, 4am-12am; Fri, 4am-6:45 pm; Sat, 12pm-12am Egged bus #475 runs from the new Tel-Aviv Central Bus Station to Ben-Gurion Airport Platform #3.

Weekdays, 6am-11:30 pm

Railway Access. Shuttle service - (an Israel Airports Authority bus will make rounds between terminal 3 and terminals 1 & 2 at times corresponding with the train timetable).

Nearest station: Tel-Aviv - Central

Address: Al Parashat Derachim st. Arlozorov st.

Railway information service

Tel. 03-5774000 and *5770

from any phone + Pele-phone & Cellcom users .

The service is available Sunday - Thursday between 6:00 a.m.-11:00 p.m.

Fridays between 6:00 a.m. - 3:00 p.m.

Saturday evening from departure of the first train - 24:00 p.m.

Public Transportation

The bus is an efficient and inexpensive way to travel in Israel, offering a comfortable and air-conditioned ride. Buses to all points operate daily except on Friday from sunset, and on Saturday and Jewish holidays until sunset (shabbat). Most bus lines from just before 6am until approximately 11:45pm. Exact change is not required.

The main bus company in Israel, "Eged" – Information center 03-6948888. The local bus company in Tel-Aviv, "Dan" - Information center 03-6394444.

Taxis

It is recommended not to use random Taxi services, but to approach the Taxi dispatcher. All taxis have taximeter displayed on the dashboard. Fares have an extra addition at night and for extra luggage. Make sure that you are charged the correct price. Taxi services are regulated and the Taxi companies at BGN operate under permission.

Taxi station near the hotel.

"Hayarkon" Taxis"- 03-5223233.

"Gordon" Taxis"- 03-5272999.

Car rental

There are several international rent-a-car companies and also some local companies.

Useful Addresses and Telephone numbers

Emergency Services

Just dial the following numbers from anywhere in the country:

Police 100

Ambulance 101

Fire Department 102.

EI-AI Israel's national Airlines – 03-9716111.

Hotel: Sheraton Moriah Tel-Aviv

Hayarkon 155

Tel Aviv, 63453 IL

Telephone, 03 5216666 (The town area code is not needed within Tel Aviv)

Airport Information

(03) 971-0000

Recorded flight info in English
(03) 972-3344

ICECS 2004 Secretariat:

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Technical Program

ICECS 2004 at Glance

Sunday, December 12

Time	Tutorial	Hall
9:00 – 12:30 Morning	Circuit Techniques for Operational Amplifier Speed and Accuracy Improvement: Analog Circuit Design with Structural Methodology	Carmel
13:30 – 17:00 Afternoon	Mixed Analog/Digital Circuits in SOI CMOS	Carmel
20:00 – 21:30	Reception	Yarden Sheraton Moriah Hotel

Monday, December 13

9:00 – 9:15	Opening Remarks	Arbel & Tabor
9:15 – 9:30	Technical program overview	
9:30 – 10:30	Plenary session – G. Moschytz	
10:30 – 11:00	Coffee break	Conference entrance hall
Time	Session	Hall
11:00 – 12:40	MA1 ANALOG AMPLIFIERS	Galil
	MB1 NONLINEAR CIRCUITS	Carmel
	MC1 INTERCONNECT MODELING	Tabor
	MD1 SPECIAL SESSION: NANOELECTRONICS, NANOTECHNOLOGY, AND GIGA- SCALE SYSTEMS	Arbel
12:40 – 14:00	Lunch	

Time	Session	Hall
14:00 – 15:40	MA2 RF OSCILLATORS	Galil
	MB2 COMMUNICATION SYSTEMS	Carmel
	MC2 CMOS IMAGING SENSORS	Tabor
	MD2 SPECIAL SESSION: NEUROMORPHIC SYSTEMS	Arbel
15:40 – 16:00	Coffee break	Conference entrance hall
16:00 – 17:40	MA3 ANALOG FILTERS	Galil
	MB3 SIGMA-DELTA MODULATORS	Carmel
	MC3 HIGH PERFORMANCE INTEGRATED CIRCUITS	Tabor
	MD3 NEURAL NETWORKS	Arbel
18:00 – 18:15	Lighting of the Hanuka candles	Conference entrance hall

Tuesday, December 14

Time	Session	Hall
8:00 – 8:55	Plenary session – U. Weiser	Arbel & Tabor
9:00 – 10:40	TA1 SPECIAL SESSION: GRAND CHALLENGES IN CIRCUITS AND SYSTEMS	
	TA1.1 CHALLENGES IN ULTRA DEEP SUBMICROMETER HIGH PERFORMANCE VLSI CIRCUITS,	Galil
	TA1.2 GRAND CHALLENGES IN IMAGE PROCESSING AND ANALYSIS,	Carmel
	TA1.3 CHALLENGES IN CMOS IMAGER DESIGN,	Tabor

Time	Session	Hall
	TA1.4 GRAND CHALLENGES IN SPATIAL-TEMPORAL COMPUTING ON IMAGE FLOWS,	Arbel
10:40 – 11:00	Coffee break	Conference entrance hall
11:00 – 12:40	TA2 CONVERSION CIRCUITS	Galil
	TB2 VIDEO AND MULTIMEDIA TECHNOLOGY	Carmel
	TC2 PROCESS AND DEVICE SIMULATION	Tabor
	TD2 BIOMEDICAL AND INDUSTRIAL APPLICATIONS	Arbel
12:40 – 14:00	Lunch	
14:00 – 15:40	TA3 POWER ELECTRONICS	Galil
	TB3 MIXED-SIGNAL CIRCUITS	Carmel
	TC3 SYSTEM AND DEVICE MODELING	Tabor
	TD3 CONTROL SYSTEMS AND APPLICATIONS	Arbel
15:40 – 16:00	Coffee break	Conference entrance hall
16:00 – 17:40	TA4 ANALOG CIRCUITS AND APPLICATIONS	Galil
	TB4 COMMUNICATION RECEIVERS	Carmel
	TC4 INTERCONNECT DESIGN	Tabor
	TD4 MICRO-OPTO-ELECTRO-MECHANICAL SYSTEMS	Arbel

19:45 – 22:30

Banquet

Yarden

Wednesday, December 15

Time	Session	Hall
8:00 – 8:55	Plenary session – P. (Chung-Yu) Wu	Arbel & Tabor
9:00 – 10:40	WA1 ANALOG FILTERS	Galil
	WB1 SIGMA-DELTA MODULATORS	Carmel
	WC1 HIGH PERFORMANCE INTEGRATED CIRCUITS	Tabor
	WD1 NEURAL NETWORKS	Arbel
10:40 – 11:00	Coffee break	Conference entrance hall
11:00 – 12:40	WA2 HIGH PERFORMANCE ARCHITECTURES	Galil
	WB2 DIGITAL SIGNAL PROCESSING	Carmel
	WC2 SEQUENTIAL SYNTHESIS METHODOLOGIES	Tabor
	WD2 IMAGE PROCESSING	Arbel
12:40 – 14:00	Lunch	
	WA3 ADVANCED SYNTHESIS AND VERIFICATION METHODOLOGIES	Galil
14:00 – 15:40	WB3 VLSI CRYPTOLOGY	Carmel
	WC3 LOW NOISE AMPLIFIERS AND ADAPTIVE PROCESSING	Tabor
15:40 – 16:00	Coffee break	Conference entrance hall

Plenary sessions

Plenary session:

Monday, December 13

Time: 9:30 – 10:30

Hall: **Arbel & Tabor Hall**

George S. Moschytz- Bar-Ilan University, Israel, Swiss Federal Institute of Technology Zürich (ETH)

From LC Filters to Filters-on a-Chip: A Technological Odyssey.

Summary and Short Outline:

The beginning of the evolution of circuits and systems from discrete-component breadboards to integrated circuit chips goes back more than forty years. One of the last holdouts in this development was that of frequency-selective inductor-capacitance (LC) filters, because the three-dimensionality of inductors defied integration on a chip. The fact that continuous-time frequency-selective filters can be integrated today, as part of so-called mixed-mode systems on a chip, is the result of decades of development and experimentation in an effort to substitute the electromagnetic resonance effect by inductorless active circuits. That this is today possible on-chip is the culmination of numerous ingenious developments ranging from the early thin-film and thick-film hybrid active-RC filters, to digital and switched-capacitor filters, to today's on-chip-integrated, continuous-time, active RC filters. The long odyssey from then to now involved extraordinary theoretical and technological developments that will be described briefly in this talk. It will be shown that although this development is not yet over, today's filters-on-a-chip far exceed anything that could have been dreamt of forty years ago.

Short Biography:

George S. Moschytz (M.65-SM.77-F.78) received the E.E. Diploma and the Ph.D. degree from the Swiss Federal Institute of Technology (ETH), Zurich, in 1958 and 1962, respectively. From 1960 to 1962, he was with RCA Laboratories, Zurich. From 1963 to 1972, he was with Bell Laboratories, Holmdel, NJ, where he developed and later supervised methods of designing hybrid-integrated active RC filters and silicon-integrated logic circuits. From 1973 till 2001 he was Professor of Network Theory and Signal Processing and Director of the Signal and Information Processing Laboratory at ETH in Zurich. In 2001 he joined the Bar-Ilan University in Israel, where he is head of a new Department for Electrical and Computer Engineering. He has authored and co-

authored more than 250 papers in the field of network theory, active and switched-capacitor filter and network design, and sensitivity theory, holds numerous patents, and is author and co-author of over ten books in these and related areas. His present interests are analog, digital, switched-capacitor, switched-current, and adaptive filters, cellular neural networks and wavelets for signal processing, and the application of signal processing techniques to medical problems and bio-signals. Prof. Moschytz is Past-President of the IEEE Swiss Chapter on Digital Communication Systems and a Member of the Swiss Electrotechnical Society.

From 1981 to 1982, he was President of the Swiss Section of the IEEE and served several terms in the Adcom of the IEEE Circuits and Systems Society. He has been on the Editorial Board of the Proceedings of the IEEE and was an Associate Editor of the IEEE Circuits and Systems Magazine. He was on the Board of Governors of the IEEE Circuits and Systems Society and was President of the Society in 1999. He is an elected member of the Swiss Academy of Engineering Sciences, winner of the Best Paper Award (for a paper on active filter design using tantalum thin-film technology), winner of the IEEE CAS Education Award, and has been awarded the IEEE Millennium Medal, the IEEE Circuits and Systems Society Golden Jubilee Medal, and is a member of Eta Kappa Nu.

Plenary session:

Tuesday, December 14

Time: 8:00 – 8:55

Hall: **Arbel & Tabor Hall**

Uri Weiser- Intel Corporation, Technion, Haifa, Israel

Microprocessors: Bypass the power wall (at least for a while)

Summary and Short Outline:

Staying within Microprocessor power envelope, becomes a major design obstacle in the design of future high-end Microprocessors.

A new paradigm should be introduced to enable continues rapid performance improvement (Moore's law). This talk will introduce a solution that was carved without breaking the law of physics. The solution will reach better performance by narrowing the application range. The performance power curves and parameter will be presented.

Short Biography:

Uri Weiser received his B.Sc and M.Sc degrees in Electrical Engineering from the Technion, Israel Institute of Technology, Haifa, Israel in 1970 and 1975 respectively. He received his Ph.D in Computer Science from the University of Utah, Salt Lake City, in 1981.

Dr. Weiser joined Intel in 1988. Since then he held various positions at Intel among them: Director of Intel s processor s strategy, Co-manger of Austin Design Center, Director of Streaming architecture and more. Uri initiated the PentiumŽ processor concept definition, feasibility study and performance simulator, drove the definition of Intel's MMX technology architecture, co-invented the "Trace-Cache" concept, the "Streaming data concepts", "Dynamic tuning", and others.

Prior to his career at Intel, Dr. Weiser worked for the Israeli Department of Defense (RAFAEL) from 1970 to 1984, as Research and System Engineer. His next position was with National Semiconductor Design Center, Israel from 1984 to 1988, leading the design of National's NS32532 Microprocessor. Dr. Weiser became an Intel Fellow in 1996 and got the IEEE Fellow title in 2002 "for contributions to Computer Architecture". He got the Distinguish Fellow of the Electrical Engineering Department, Technion in 2004. Dr. Weiser holds an Adjunct Associate Professor position at the Technion IIT, he is an Associate Editor of IEEE Micro of Architecture Letters.

Plenary session:

Wednesday, December 15

Time: 8:00 – 8:55

Hall: **Arbel & Tabor Hall**

Peter (Chung-Yu) Wu, National Chiao Tung University

Nanometer Era: 90-nm/65-nm Design Technologies and Beyond

Summary and Short Outline:

Moore's Law applies to scaling of silicon chips into the Nanometer Era. It will steadily continue into sub-10nm regime. This talk will address research and development details in 90-nm and 65-nm technology nodes with advanced data from world-leading foundries such as TSMC, UMC, and academic institutions. Design issues and emerging solutions for (A) analog and mixed-signal designs, (B) memory design, and (C) digital ASIC design will be presented. Key issues such as power consumption, design-for-manufacturability, yield enhancement, will be addressed. Recent developments in non-silicon nano-devices will also be described. A closer look into 45-nm technology node and beyond will be presented. When the modern CMOS technology was scaled to the 90 nm node by breaking the "100 nm brick wall" a few years ago, the Nanometer Era for silicon chips began. In the Nanometer Era, there are numerous challenges and opportunities in the research fields of process technologies, devices, circuits, systems, and electronic design automation (EDA). According to Moore's Law, nano-CMOS mass-production technology will continue to advance till around 2020 where sub-10-nm technology node could be reached. Then non-silicon nanostructures will take over afterward. Currently, world-leading foundries such as TSMC and UMC have provided mature 130-nm and 90-nm technologies. They are preparing 65-nm technology for mass production. Moreover, advanced research on 45-nm technology and beyond is extensively conducted. Key technology developments from the foundries will be highlighted.

In the post-silicon areas, the device/structure portfolio has many interesting targets including carbon-nanotube, quantum-dot, spintronics, molecular electronics, nano-bionics, single electronics, etc. The grand challenges are:

- (1) Reliable signal input/output and interconnection for nano-devices / nanostructures;
- (2) Stable, reproducible, and low-cost nanofabrication process for mass production with reasonable yield;

- (3) New nanoelectronic circuits, systems, architectures, and design methodologies for nano-integration;
- (4) Verification, testing, and packaging methods for nano-system chips;
- (5) Fundamental quantum physics in the atomic or molecule level.

At the 90-nm node of CMOS, the power supply voltage is round 0.9 V. In the year of 2016 or sooner, the 22 nm node will be reached with the use of 0.4 V supply voltage. Despite the complicated device characteristics involving quantum effects at all sub-65 nm nodes, the grand challenges for silicon nanoelectronics are in five major aspects: (1) Interconnect modeling and designing: Interconnect occupies over 75% of signal delay at 90 nm or smaller nodes and requires efficient modeling techniques and revolutionary chip design methodology; (2) Ultra-low-power (ULP) low-voltage (LV) but high-speed high-frequency analog/digital IPs: Sub-1 V ULP LV GHz analog/digital intellectual properties (IPs) which can migrate over 3 or more technology generations without substantial redesign efforts are required; (3) Programmability in IP/whole-chip design and verification: Highly programmable IPs and System-on-Chips (SoCs) are needed to avoid the expensive masks/chips redone and increase the design flexibility; (4) Embedded software to make SOC meet future needs in many major intelligent applications; (5) Fast design cycles: Can we design an 100-billion-transistor SOC within 100 days or less?

The great impacts of the above design challenges on (A) analog and mixed-signal design, (B) memory design, (C) digital ASIC design, and (D) EDA will be described. The current development status of IC design industry in Taiwan and worldwide will be presented with detailed data. Finally, perspectives will be given.

Short Biography:

Dr. Peter (Chung-Yu) Wu (1998 IEEE Fellow) is Centennial Chair Professor and also Dean of EECS College at National Chiao Tung University. He serves as VP-Conferences for 2004 -2005, and was a BoG member in IEEE CAS Society in 2003. He was General Chair of 1994 IEEE APCCAS Conference. Dr. Wu served as Guest Editor of Aug. 1997 Multimedia Special Issue for IEEE Trans on CSVT, as Associate Editor for Trans. on CAS-Part II, Trans. on VLSI Systems, and Trans. on Multimedia. He currently serves as CAS Editor for IEEE Circuits and Devices Magazine. Dr. Wu is the founding Chair of Technical Committee on Nanoelectronics and Giga-scale Systems. He served as Chair of Neural Technical Committee, as Chair of Multimedia Technical Committee. He is CAS Representative to IEEE Neural Networks Society. In regional activities area, Dr. Wu served as CAS Taipei Chapter Chair, and IEEE Taipei Section Chair. In 2000-2001, Dr. Wu served as a Distinguished Lecturer in IEEE CAS Society.

Dr. Wu is a recipient of IEEE Third Millennium Medal, a Fellow of IEEE, and also a U.S. Fulbright Scholar. He is a member of Eta Kappa Nu and Phi Tau Phi Honorary Scholastic Societies. He served as a Semester-Full Professor in Fall 2003 and as Adjunct International Professor since Spring 2004 for the ECE Department at University of Illinois, Urbana.

Tutorials

Morning Tutorial

Sunday, December 12

Time: 9:00 – 12:30

Hall: Carmel

Vadim V. Ivanov - Texas Instruments, Inc

I. M. Filanovsky - University of Alberta, Canada

Circuit Techniques for Operational Amplifier Speed and Accuracy Improvement: Analog Circuit Design with Structural Methodology

Summary and Short Outline:

OpAmp is the main analog building block for both the systems on discrete elements and systems on silicon. The parameters of OpAmp often define and limit the overall system performance. CMOS technology provides an opportunity to use more complex structural solutions and circuit techniques to improve OpAmp accuracy, power/speed ratio, add new functional advantages, like low voltage supply operation capability or rail to rail input without switching point, for negligible additional component cost. The circuit techniques that will be demonstrated during this course were proven in design of leading industrial OpAmps. These techniques are unified by a common structural design approach, based on the following principles:

- system analysis at the high level of abstraction using the graphic tools like signal flow graphs, and generation of the set of equivalent graph modifications,
- equivalent graph transformations to the form when every important parameter in the system or amplifier is controlled by a dedicated feedback loop;
- stability of these loops is achieved without compensation capacitors, using one-stage (preferably current) amplifiers,
- system synthesis consists of implementation of the set of the gain structure modifications followed by simulations based on available library of cells, and selection of the best circuit solutions.

The particular topics covered in this half-day course include:

- amplifier speed and correct number of the gain stages;
- gain boosting in single and two-stage OpAmp structures and elimination of gain erosion due to the drain-body leakage in single-well process;
- design of rail-to-rail input stages:

NMOS/PMOS stages with stabilized transconductance,

- PMOS stage with low-noise charge pump for the tail current source,
Using the low-V_t transistors to eliminate the switching point;
- CMR and PSR improvement:
 - design of high quality tail current source,
 - cascoding of the input pair,
 - class AB output stage design;
 - slew rate boost techniques;
 - overload recovery time improvement;
 - design techniques for 0.9 V power supply;
 - using advantages of modern processes implementing different types of transistors.

Short Biographies:

Vadim V. Ivanov

Dr. Vadim Ivanov has his MSEE in 1980 and Ph.D. in 1987, both from the Institute of Electrical Engineering, St. Petersburg, Russia. He worked as the designer of electronic systems and ASICs for naval navigation equipment from 1980 to 1991 in St. Petersburg, and as the designer of mixed signal ASICs for sensors, GPS/GLONASS receivers and motor control systems between 1991 and 1995. Dr. Ivanov joined Burr Brown (presently Texas Instruments, Tucson) in 1996 as a senior member of technical staff, where he is involved with the design of operational, instrumentation, power amplifiers, references and switching and linear voltage regulators. Dr. Ivanov has 25 US patents, with 10 more pending, on analog circuit techniques. He is the author and coauthor of more than 30 technical papers and three books: "Integrated Power Amplifiers" (Leningrad, Rumb, 1987), "Analog System Design with ASICs" (Leningrad, Rumb, 1988), both in Russian, and "Operational Amplifier Speed and Accuracy Improvement", Kluwer, 2004.

I. M. Filanovsky

I. M. Filanovsky (M'81-SM'90) was born in Kirov, USSR, in 1940. He received the M.Sc. degree in 1962 and the Ph.D. degree in 1968, both in electrical engineering from V. I. Ulianov (Lenin) Institute of Electrical Engineering, Leningrad, USSR.

In 1976, he joined the University of Alberta, Canada, where he is currently a Professor. He has coauthored with V.V. Ivanov the book Operational amplifier speed and accuracy improvement (Analog circuit design with structural methodology) (Kluwer Academic Publishers, 2004), and contributed to four books, Sensor Technology and Devices, L. Ristic, Ed., (Norwell, MA: Artech House, 1994), Analog VLSI: Signal and Information Processing, M. Ismail and T. Fiez, Eds, (New York: Mc-Graw-Hill, 1994), The Circuits and Filters

Handbook, W.-K. Chen, Ed., (Boca Raton, FL: CRC Press, 1995), and The Electronics Handbook, J. Whitaker, Ed., (Boca Raton, FL: CRC Press, 1996). He was also a contributor to The Encyclopedia of Electrical and Electronic Engineering, J. Webster, Ed., (New York: Wiley, 1999) and Comprehensive Dictionary of Electrical Engineering, P. A. Laplante, Ed., (Boca Raton, FL: CRC Press, 1999). In addition, he is the author or coauthor of about 200 journal and conference proceedings publications on circuit theory (theory of approximation, theory and technical applications of oscillations, strongly nonlinear oscillations) and applied microelectronics (analog electronic circuits, oscillators and multivibrators, signal-conditioning circuits for sensors). He has four patents on electronic circuits.

Dr. I. M. Filanovsky is an Associated Editor of IEEE Transactions on Circuits and Systems, Part I. He is a Professional Engineer registered with APEGGA, Alberta, Canada. In the past he was Co-chairman and Technical Program Chairman of 33rd International Midwest Symposium on Circuits and Systems in Calgary, Canada, 1990.

Afternoon Tutorial

Sunday, December 12

Time: 13:30 – 17:00

Hall: Carmel

Andreas G. Andreou - Johns Hopkins University, Baltimore, USA

Mixed Analog/Digital Circuits in SOI CMOS

Summary and Short Outline:

Silicon on silicon (SOI) is emerging as a mainstream technology poised to become the standard for deep sub-micron VLSI. Devices with $f(\text{max})$ near 100GHz have been reported in 0.18 micron CMOS fabricated on ultra-thin silicon on insulator. Ultra-thin silicon on sapphire (SOS) is an alternative to silicon/silicon dioxide based technologies that employs epitaxially grown ultra-thin silicon and SIMOX isolation to form individual device islands. The absence of a conductive substrate and hence parasitic capacitances as well as excellent device characteristics at low frequencies makes this technology very attractive for high speed digital and radio frequency circuits and systems on a chip. The optical transparency of the sapphire together and its excellent thermal properties make ultra-thin silicon on sapphire an excellent candidate for system on a chip optoelectronics (SOCOE).

In this lecture we introduce the basic SOS technology and discuss the design of mixed analog/digital circuits in ultra-thin silicon on sapphire. We address traditional tradeoffs and present solutions to problems arising from the insulating substrate. Furthermore we expand on design perspectives and design methodologies that pertain to the ultra-thin SOS process that offers CMOS transistors with three different threshold voltages for each type of device. We make the discussion concrete by focusing on the design of high speed optoelectronic circuits, low power functional blocks that exploit the unique properties of this technology, amplifiers, data converters, active pixel sensor and event based imagers, sensor readout and biomedical telemetry. We will also discuss work towards surface micromachined MEMS structures in the same technology.

Short Biography:

Andreas G. Andreou

Andreas G. Andreou received his Ph.D. in electrical engineering and computer science in 1986 from Johns Hopkins University. Between 1986 and 1989 he held post-doctoral fellow and associate research scientist positions in the electrical and computer-engineering department while also a member of the

professional staff at the Johns Hopkins Applied Physics Laboratory. Andreou became an assistant professor of electrical and computer engineering in 1989, associate professor in 1993 and professor in 1996. In 1995 and 1997 he was a visiting associate professor and visiting professor respectively in the computation and neural systems program at the California Institute of Technology. In the summer of 2001 he was a visiting professor at Tohoku University in Japan working on 3D integration. He is also a faculty in the Whitaker Biomedical Engineering Institute at Johns Hopkins University and founding director of the Whitaker Institute fabrication and lithography facility. He is a recipient of a National Science Foundation Research Initiation Award and he is the co-founder of the Center for Language and Speech Processing at Johns Hopkins University. He is the recipient of the 2000 IEEE Circuits and Systems Society Darlington Award. Between 2000 and 2003 he served as a Member of the Board of Governors for the CAS Society.

Andreou's research interests include integrated circuits, sensory information processing and neural computation. He is a co-editor of the Kluwer Academic Publishers book: Adaptive Resonance Theory Microchips, 1998. He is associate editor of the IEEE Transactions on Circuits and Systems: Express Letters.

Paper Presentations

MA1: ANALOG AMPLIFIERS

Monday, December 13

Time: 11:00 – 12:40

Hall: Galil

Chair: **C. F. Tai**, Taiwan University, Taipei, Taiwan

MA1.1

A NEW CONFIGURATION OF TWO-STAGE WIDE-BAND AMPLIFIER WITH MATCHED INPUT AND OUTPUT IMPEDANCES, *I. Filanovsky, **A. Sachko, **J. Long, *University of Alberta, Edmonton, Canada, TU Delft, Netherlands.

The proposed amplifier is a modification of two-stage Meyer-Blauschild configuration. Through the use of two independent bias current sources and an interstage buffer, design of ac parameters such as input impedance, gain, and output impedance become independent. In addition, the bias and ac parameter design are loosely coupled in the new amplifier. This allows one to develop a new approach to the design of wide-band amplifiers similar to that of systems with operational amplifiers.

MA1.2

A BULK-DRIVEN CMOS OTA WITH 68 DB DC GAIN, J. Rosenfeld, M. Kozak, E. G. Friedman, University of Rochester, Rochester, NY, USA.

An ultra-low voltage rail-to-rail operational transconductance amplifier (OTA) based on a standard digital 0.18 micrometer CMOS process is described in this paper. Techniques for designing a 0.8 volt fully differential OTA are discussed including bias and reference current generator circuits. To achieve rail-to-rail operation, complementary input differential pairs are used, where the bulk-driven technique is applied to reduce the threshold limitation of the MOSFET transistors. The OTA gain is increased by using auxiliary gain boosting amplifiers. This additional circuitry enables the OTA to operate at 0.8 volts, achieving an open loop gain of 68 dB while consuming 94 microW. The DC gain of the amplifier is the highest gain achieved to date in bulk-driven amplifiers.

MA1.3

A 100 DB CMRR CMOS OPERATIONAL AMPLIFIER WITH SINGLE-SUPPLY CAPABILITY, I. Filanovsky, V. Ivanov, J. Zhou, University of Alberta, Edmonton, Canada

A CMOS operational amplifier that has a 100 dB CMRR is described. This is achieved combining the high output impedance tail current source with control of the drain-source voltage of input transistors. Common-mode input signal range includes negative rail voltage. This is obtained applying the controlled bulk bias of both input and cascoding transistors. The amplifier consists of two gain stages connected via cascoded current mirror with the voltage gain boost. The suppression of impact ionization current in the output stage improves gain by more than 20 dB.

MA1.4

TWO NOVEL CROSS-CASCADE DIFFERENTIAL AMPLIFIERS, Y. Bruck, M. Zelikson, IBM, Haifa, Israel.

Two novel cascode circuits, the Differential Cross-Cascode and Differential Cross-Follower, is proposed and investigated. In the circuits input signal voltage being applied simultaneously to the inputs of common emitter/source and common base/gate stages, and besides the inputs of CE/CS and CB/CG being cross-coupled. We show that the input signal is amplified in the input circuit, furthermore the input impedance and the current gain increase considerably and the bandwidth is essentially expanded. Simulation results of such a cascode are presented. The obtained bandwidths (18.7 GHz) to be more than twice as wide as compared with the bandwidth of the ordinary cascode (8.6 GHz).

MA1.5

A WIDE-LINEAR RANGE SUBTHRESHOLD OTA BASED ON FGMOS TRANSISTOR, A. El Mourabit, P. Pittet, G. N. Lu, University of Claude Bernard, Lenac, France.

This paper presents a new configuration of linear CMOS subthreshold operational transconductance amplifier (LSOTA) working at 1.5V with very low power consumption. Based on FGMOS technique, the developed OTA has a wide input range and small G_m , suitable for implementing low frequency analog and monolithic continuous-time filters. For demonstration a low pass second order filter was designed and simulated. The power consumption of the filter is less than 21W and the topology achieves 76 dB linearity for fully balanced input dynamic range up to 1 V_{pp} at 1.5V supply voltage.

MB1: NONLINEAR CIRCUITS

Monday, December 13

Time: 11:00 – 12:40

Hall: Carmel

Chair: **S. Engelberg**, Jerusalem College of Technology, Israel.

MB1.1

NONLINEAR DYNAMICS OF FIRST-ORDER DPLL WITH FM INPUT AND

PHASE DETECTOR DC OFFSET, B. O'Donnell, P.I. Curran, University College Dublin, Dublin, Ireland.

Phase-locked loops are important engineering systems. In previous work the nonlinear dynamics of a first order digital phase-locked loop (DPLL) with frequency modulated input and small values of modulating frequency were considered. In this paper the effect of a phase detector DC offset on the behavior of the loop and in particular its lock range is explored. A modulated input to the system causes a perturbation of the fixed-point in the lock region and results in a uniform scatter or a 'belt' of points for this region. The bifurcation properties of these 'belts' are distinct numerically from the fixed-point approach.

MB1.2

THE CENTRAL LIMIT THEOREM AND LOW-PASS FILTERS, S. Engelberg, Jerusalem College of Technology - Machon Lev, Jerusalem, Israel.

The result of connecting many low-pass filters in series is considered. It is shown that if the impulse response of the filters is non-negative, then a version of the central limit theorem applies. Making use of the central limit theorem it is shown that as the number of filter sections gets large the total delay of the cascaded filter system tends to the sum of the (approximate) time delays of each of the filters. Using examples, it is shown that the rate at which the impulse response converges to a Gaussian is dependent on the nature of the impulse responses of the constituent low-pass filters.

MB1.3

MATHEMATICAL PROGRAMMING AND RESISTOR TRANSFORMER

DIODE NETWORKS, N. Harihar, IIT Bombay, Mumbai, India.

In this paper we present results for networks with ideal transformers, conical diodes and resistors which are conical analogues of vector space based fundamental results for networks with ideal transformers and resistors. By a

conical diode we mean a device which satisfies $v_D \leq 0, i_D \geq 0$, where v_D, i_D represent the voltage and current associated with the device. We show: 1. if we connect ideal transformers and conical diodes resulting in a 'Transformer Diode multiport' (TD-multiport) the permissible voltage vectors and current vectors at the exposed ports form complementary polar cones and 2. if we connect across the ports of a TD-multiport a $1/\Omega$ resistor in series with a voltage source E_{i} for the i^{th} port (for each i), then the voltage vector appearing across the ports of the multiport would be the projection of the voltage source vector \mathbf{E} onto the port voltage cone of the multiport.

MB1.4

A NEW METHOD TO IMPROVE THE IMPEDANCE OF THE CC-II'S X INPUT, L. N. Alves, R. Aguiar, University of Aveiro, Aveiro, Portugal.

This paper presents a new method to improve the CC-II's X input impedance. The new method applies a double feedback scheme comprising both series-shunt negative and series-series positive feedback paths. This method achieves input impedance levels below $-15\text{dB}\omega$ (in comparison to other reported methods), with controlled frequency peaking. Simulation results compare frequency performance of the proposed method with other reported methods, using the same reference CC-II. Effects of feedback on current and voltage transfers of the CC-II are also discussed, pointing to limitation factors on impedance reduction.

MB1.5

NEW CHAOTIC THIRD-ORDER LOG-DOMAIN OSCILLATOR WITH TANH NONLINEARITY, A. Ascoli, P. Curran, O. Feely, University College Dublin, Dublin, Ireland.

Log-domain filters are an intriguing form of current-mode circuit in which the large-signal exponential current-voltage relationship of the bipolar junction transistor is used first to convert the input currents to logarithmic form, where the analog processing takes place, and then to map the output voltage waveforms back to the current domain at the end of the filtering process. The log-domain filter synthesis technique can be extremely useful in the design of chaotic oscillators suitable for low-power high-speed integrated circuit implementations. This paper presents a new third-order log-domain chaotic oscillator, which may be used in chaos-based communication systems. Although the design of the proposed oscillator stems from a known nonlinear dynamical system which may be subject to chaotic oscillations, its dynamics differ from those of the model and, as a result, are worth investigating.

MC1: INTERCONNECT MODELING

Monday, December 13

Time: 11:00 – 12:40

Hall: Tabor

Chair: **A. Kolodny**, Technion, Haifa, Israel.

MC1.1

ELECTROMIGRATION-DEPENDENT PARAMETRIC YIELD ESTIMATION,

*R. Barsky, **I. A. Wagner, *Technion, Haifa, Israel, **IBM, Haifa, Israel.

We define and investigate the problem of electromigration faults caused by spot defects during VLSI manufacturing process. Analysis is given for a simple layout, and simulations are presented and discussed for a more complicated case. It is shown that in some cases, electromigration-dependent parametric faults can make a significant contribution to the total yield estimation.

MC1.2

REPEATER INSERTION COMBINED WITH LGR METHODOLOGY FOR ON-CHIP INTERCONNECT TIMING OPTIMIZATION,

M. Moreinis,
A. Morgenshtein, I. Wagner, A. Kolodny, Technion, Haifa, Israel.

Combination of Repeater Insertion with novel LGR (Logic Gates as Repeater) technique is presented, providing a methodology for delay optimization of CMOS logic circuits with RC interconnects. The traditional interconnect segmentation by insertion of repeaters is generalized to segmentation by distributing logic gates over interconnect lines and adding a reduced number of repeaters. Expressions for optimal segment length, optimal number of additional repeaters and scaling factors for both gates and repeaters are derived. An iterative solution is presented. Optimization results for several circuits are presented, showing significant improvement in performance in comparison with traditional repeater insertion.

MC1.3

3D POWER GRID MODELING,

Y. Yagil, L. Zlydina, Intel Corporation, Haifa, Israel.

The paper describes on-chip 3D power grid (PG) modeling for high performance CPU designs. We show that for high frequencies (above 1 GHz) one has to use full RLM PG model with extracted partial self and mutual conductor's inductances, rather than resistive R or RL models. We also present a practical model reduction technique named "real space reduction" (RSR), which permits to simplify the model and reduce memory and simulation time without significant accuracy losses.

MC1.4

PULSE-FORMING REACTANCE NETWORK SHAPES A QUASI-RECTANGULAR PULSE FROM SINUSOIDAL VOLTAGE, I. M. Filanovsky, X. Dong, University of Alberta, Alberta, Canada.

The paper describes synthesis of a pulse-forming reactance network that shapes a quasi-rectangular voltage pulse at a resistive load when the source of sinusoidal voltage connected to the network is turned on. The derivative of the output pulse voltage is described by positive and delayed negative semi-periods of sine-squared function. The real and imaginary parts of the Laplace transform of this pulse are expanded in infinite products. Then, using a finite number of terms in these products one can obtain the transfer function realizable as a reactance network loaded by resistor.

MC1.5

MODELING OF INTEGRATED MONOLITHIC TRANSFORMERS FOR SILICON RF IC, O. El Gharniti, E. Kerherve, J. B. Begueret, P. Jarry, University of Bordeaux, Bordeaux, France.

We present a compact and scalable model for on-chip transformers fabricated in silicon IC technology. The model is driven from the layout and the process technology specifications. It is suitable for design optimization and circuit simulation. EM-simulation is used to validate the model. The proposed model shows excellent agreement with EM-simulation over a large frequency range (1-15GHz).

MD1: SPECIAL SESSION - NANOELECTRONICS, NANOTECHNOLOGY, AND GIGA-SCALE SYSTEMS.

Monday, December 13

Time: 11:00 – 12:40

Hall: Arbel

Chair: **P. (Chung-Yu) Wu**, National Chiao Tung University, Taiwan.

MD1.1

A LOW POWER DESIGN ON DIFFUSIVE INTERCONNECTION LARGE-NEIGHBORHOOD CELLULAR NONLINEAR NETWORK FOR GIGA-SCALE SYSTEM APPLICATIONS, S. Chen, C. Y. Wu, National Chiao Tung

University, Hsinchu, Taiwan

In this paper, the diffusive interconnection large-neighborhood cellular nonlinear network (LN-CNN) with low power dissipation and small chip area is proposed and analyzed. In the proposed new architecture, the number of gain blocks can be reduced by merging template A model and template B model together with suitable adjustment. All the gain blocks are based on simple current-mirror circuits so the cell has small chip area and save more power. Thus the new architecture and circuits are suitable for large array LN-CNN implementation for giga-scale system applications. The functions of LN-CNN are verified by HSPICE simulation and the LN-CNN chip will be fabricated to verify the simulation results.

MD1.2

A LEARNABLE SELF-FEEDBACK RATIO-MEMORY CELLULAR NONLINEAR NETWORK (SRMCNN) WITH B TEMPLATES FOR ASSOCIATIVE MEMORY APPLICATIONS, ^{***}J. L. Lai, ^{**}C. Y. Wu, ^{*}National

Chiao Tung University, Hsinchu, Taiwan, ^{**}National United University, Miao-Li, Taiwan

A self-feedback ratio-memory cellular nonlinear network (SRMCNN) with the B template and the modified Hebbian learning algorithm to learn and recognize the image patterns is proposed and analyzed. In the proposed SRMCNN, the coefficients of space-variant B templates are determined from the exemplar patterns during the learning period. The weights are the ratio of the absolute summation of its neighborhood weights in the B templates was stored in the associative memory. This SRMCNN can recognize the learned patterns with distinct white-black noise and output the correct patterns. The Matlab and HSPICE software has been simulated the operation of the proposed SRMCNN. It is shown that the 18×18 SRMCNN can successfully learned and recognized 8 incompletely noisy patterns. As compared to other learnable CNN as associate

memories, the proposed SRMCNN could improve pattern learning and recognition capability. The architecture can be implemented in nano-CMOS technology for giga-scale learning system in the real-time applications.

MD1.3

VLSI IMPLEMENTATION OF THE UNIVERSAL 2-D CAT/ICAT SYSTEM, R. J. Chen, J. L. Lai, National United University, Miao-Li, Taiwan

The VLSI implementation of the universal two-dimensional (2-D) cellular automata transform (CAT) as well as inverse CAT (ICAT) is present in this paper. The universal 2-D CAT/ICAT chip is based on the 2-D CAB generator. To facilitate the development of a universal 2-D CAB generator, we adopted a CA cell structure with programmable additive rules to generate 1-D CAB first, and then utilized the canonical products of 1-D CAB to perform the 2-D CAB. We have accomplished simulations of the universal 2-D 8X8 CAT/ICAT chip by using CANDENCE tools. We also have completed the circuit synthesis of the 2-D CAT/ICAT chip by using the SYNOPSE tools with the TSMC 0.35um CMOS data-path cell-library. The maximum operation frequency was 120 MHz, and the area size was 6.8225 mm². It shows that the architecture of the proposed universal 2-D CAT/ICAT is suitable for VLSI realization.

MD1.4

OPTIMAL STRUCTURE OF INTERCONNECTION LINES FOR GHZ GIGA-SCALE NANO-CMOS SYSYTEM-ON-CHIP DESIGN, *C. Y. Wu, **J. C. Wang, *National Chiao Tung University, Hsinchu, Taiwan, **Chip Implementation Center, National science Council, Hsinchu, Taiwan

As CMOS technology is scaled down to below 90 nm, interconnection lines on a complicated chip play a very key role in speed/frequency and performance. The conventional coplanar interconnection structure has good high-frequency performance, but the chip area is large. This will significantly increase chip area of a complicated System-On-Chip (SOC) which require many interconnection lines. In this research, the optimal structure of interconnection lines for nano-CMOS technology with multi-layer metals is proposed and analyzed. It is found from simulation results that multi-layer non-coplanar interconnection lines with signal line at the top layer metal and ground line at a lower layer metal without planar space between lines have the optimal performance of transmission loss, frequency response, and chip area. Experimental chip will be designed to verify the simulation results. The proposed new interconnection structure can be applied to nano-CMOS SOC design.

MD1.5

SPINTRONIC LOGIC CIRCUIT DESIGN FOR NANOSCALE

COMPUTATION, * J. Chen, ** W.Chao, ** Q.W. Shi, *Brown University, Providence, RI, USA, ** University of Science and Technology, Beijing, China

Spintronic is an emerging multidisciplinary field and its central theme is how to actively manipulate spin polarities in solid state systems.

MA2: RF OSCILLATORS

Monday, December 13

Time: 14:00 – 15:40

Hall: Galil

Chair: **I. Filanovsky**, University of Alberta, Canada.

MA2.1

A 6GHZ LOW-NOISE QUADRATURE COLPITTS VCO, *M. Chu, D. Allstot, University of Washington, Seattle, WA, USA.

A 6GHz low-noise quadrature Colpitts VCO is presented. Use of the Colpitts configuration together with a series-injection scheme for quadrature signal generation ensures low phase noise operation. The QVCO achieves a simulated average phase noise of -140.5dBc/Hz at 3MHz offset across a 500MHz tuning range while dissipating 20mW of power. The 500MHz tuning capability is obtained using switched capacitor arrays and accumulation-mode NMOS varactors. The phase error of the QVCO is 0.55°. The figure-of-merit (FOM) and the power-frequency-tuning normalized FOM (PFTN-FOM) are 194dBc and -2dB, respectively.

MA2.2

DESIGN CONSIDERATIONS FOR ANTI-PHASE INJECTED QUADRATURE VOLTAGE CONTROLLED OSCILLATORS, *M. Chu, *S. Shekhar, *D. Allstot, **T. Bhattacharyya, *University of Washington, Seattle, Washington, USA, **Indian Institute of Technology, Kharagpur, India.

The performance of the series cascode-injected quadrature voltage-controlled oscillator (CI-QVCO) topology is compared against its degeneration-injected counterpart (DI-QVCO) based on analyses of start-up loop gain, oscillation frequency, phase noise, tuning range, and quadrature phase error. Detailed analyses and extensive simulations show that in addition to offering comparable quadrature phase error performance, the DI-QVCO configuration exhibits superior phase noise performance, more robust start-up characteristics, and greater suitability for high frequency applications that require a relatively large tuning range.

MA2.3

A MULTI-TANK LC-OSCILLATOR, C. Samori, L. Romano, S. Levantino, A. Bonfanti, A. Lacaita, Polytechnic of Milan, Milan, Italy.

This paper proposes a novel oscillator topology in which N LC tanks are coupled by active transconductors. Phase noise is shown to scale down by N, at the expense of higher power dissipation and area consumption. This

topology allows to trade-off noise and power beyond the practical limits dictated by conventional LC tank oscillators. The theoretical analysis is supported by behavioral and transistor-level simulations.

MA2.4

DIFFERENTIAL TUNING OSCILLATORS WITH REDUCED FLICKER NOISE

UPCONVERSION, C. Samori, S. Levantino, A. Bonfanti, L. Romano, A. Lacaita, Polytechnic of Milan, Milan, Italy.

The adoption of differential tuning in oscillators provides cancellation of common-mode disturbances and thus, it is expected to lower phase noise and power supply pulling. However, the direct application of differential tuning increases the capacitor non-linearity and in turn, it can raise the flicker-induced phase noise. This upconversion mechanism based on non-linearities is quantitatively assessed and a modified configuration circumventing this phenomenon is proposed and applied to the design of a 1.8-GHz LC oscillator in 0.35- μm CMOS technology. The simulated $1/f^3$ phase noise is reduced by 20 dB, without impairing tuning range and supply pulling.

MA2.5

ANALYSIS AND DESIGN OF A DUAL BAND RECONFIGURABLE VCO, *A.

Mazzanti, **P. Uggetti, **R. Battaglia, **F. Svelto, *University of Modena e Reggio Emilia, Modena, Italy, **University of Pavia, Pavia, Italy.

A systematic approach to the design of reconfigurable LC VCOs is proposed in this paper. The focus is on the choice of the reactive element of the tank most suited to switch the oscillation frequency. The optimum is the component that determines the tank Q. As an example, the design of GSM900/1800 VCO in a 0.13 μm CMOS technology, switching a series inductor, is discussed. At this frequency, the tank Q is roughly the inductor Q, and series inductor switching allows area savings with respect to parallel switching.

MB2: COMMUNICATION SYSTEMS

Monday, December 13

Time: 14:00 – 15:40

Hall: Carmel

Chair: **A. I. Perez Neira**, CTTC, Barcelona, Spain / **D. Sadot**, Ben-Gurion University, Beer-Sheva, Israel.

MB2.1

A UNIFIED FAIRNESS FRAMEWORK IN MULTI-ANTENNA MULTI-USER

CHANNELS, D. Bartolome, A. I. Perez-Neira, Telecommunications Technological Center of Catalonia (CTTC), Barcelona, Spain.

In a multi-antenna broadcast channel, the Access Point (AP) has several alternatives for distributing the scarce resources among the users. When realistic conditions are taken into account, it is not clear which is the best suited option for the AP, since there exist a trade-off between the global performance and the individual needs. In this paper, we derive an analytical framework to study fairness in a multi-antenna multi-user channel, which is useful in practical situations. Since fairness indexes in the literature usually reflect relative performances among users, we borrow ideas from portfolio selection and propose a mean vs. standard deviation analysis that allows to select a certain technique under practical conditions. We particularize this framework for a multi-antenna AP communicating simultaneously with several single-antenna terminals, and give closed-form expressions for the mean vs. standard deviation trade-off for zero forcing beamforming, dirty paper encoding, and the cooperative bound, under the assumption of a uniform power allocation among the active users. This framework can be extended to analyze other types of multi-user communications.

MB2.2

ERGODIC CAPACITY OF A 2X2 MIMO SYSTEM UNDER PHASE

UNCERTAINTY AT THE TRANSMITTER, M. Payaro, X. Mestre M. A.

Langunas, Telecommunications Technological Center of Catalonia (CTTC), Barcelona, Spain.

In this paper, we find an expression for the ergodic capacity of a 2x2 multi-input multi-output (MIMO) flat fading channel for a particular case of partial channel state information at the transmitter: we focus our study on the case where the transmitter is informed just with the modulus of the channel matrix coefficients. First, we prove that a simple power allocation strategy between transmitting antennas is the optimal scheme, in the sense that is a capacity achieving architecture. Next, we derive an expression to calculate the optimal

power assigned to each antenna, and find out that it can be expressed as a function of one of the roots of a fourth order polynomial.

MB2.3

ANALYSIS OF THE PROBABILITY DISTRIBUTION OF THE BASELINE WANDER EFFECT FOR BASEBAND PAM TRANSMISSION WITH APPLICATION TO GIGABIT ETHERNET, N. Sommer, I. Lusky, M. Miller, Texas Instruments, Herzlia, Israel.

Communication systems that employ baseband transmission (i.e. signal spectrum centered around 0 Hz) may suffer from the baseline wander (BLW) phenomenon. This phenomenon occurs when the signal has to pass through a highpass filter element in the transmission path (e.g. a transformer in the line interface). A long sequence of symbols with constant value should generate a signal with a constant level, but the signal will decay towards zero due to the highpass element. An example of a communication standard where baseband transmission is used with a DC-coupled channel is Ethernet. It can be shown that for baseband Pulse Amplitude Modulation (PAM), the baseline wander phenomenon increases the dynamic range of the signal by a factor of 2, in worst case. This increases the cost of the receiver (for example, another bit may be needed in the analog to digital converter). However, the signal will reach its extreme values with very low probability, so it seems wasteful to design for worst case. It may be more economical to design for a smaller dynamic range, but then there must be a way to understand the probability that the signal will exceed this range. This can be done by using the probability distribution of the signal in the presence of BLW, which is calculated approximately in this paper.

MB2.4

VIRTUAL INPUT QUEUED PACKET SWITCHES WITH NON-UNIFORM ARRIVALS AND BURSTY SERVICE, I. Elhanany, M. Kahane, O. Arazi, University of Tennessee, Knoxville, TN, USA.

This paper presents a performance analysis of output queued packet switch architectures employing virtual input queueing (VIQ), whereby arrival rates are non-uniformly distributed between the sources and the service intervals are bursty. In particular, we study the case of a two-state Markov-modulated service discipline, reflecting on several pragmatic scenarios such as noisy packet radio networks. We show that by exploiting an extended Markov-modulated service process and the Geo/GI/1 queueing model, closed-form expressions for the mean queueing latencies can be obtained. The methodology established in this paper can be extended to derive additional performance metrics and expected behavior of more complex packet switching architectures.

MB2.5

PERFORMANCE EVALUATION OF PSEUDO SELF-SIMILAR TRAFFIC, M. Kahane, Y. Ben-Shimol, D. Sadot, Ben-Gurion University, Beer-Sheva, Israel.

Several studies demonstrated that network traffic exhibits self-similarity and long-range dependence. Of the new methods for modeling self-similar traffic, the pseudo self-similar traffic model (PSST) is especially attractive since it is simple, has only two parameters to fit and is readily analyzed by classical queueing theory methods. In this paper we perform a performance evaluation of the PSST model by investigating its suitability to model the queueing behavior of self-similar traffic. We simulate a system fed by self-similar traffic traces with a single server and geometrically distributed service times. The observed steady state queue size distribution is compared to the one predicted by a PSST model fitted to the parameters of the traffic traces.

MC2: CMOS IMAGING SENSORS

Monday, December 13

Time: 14:00 – 15:40

Hall: Tabor

Chair: **Y. Nemirovsky**, Technion, Haifa, Israel.

MC2.1

A CMOS FOCAL-PLANE RETINAL SENSOR DESIGNED FOR SHEAR

MOTION DETECTION, W. C. Hsieh, C. Y. Wu, C. T. Chiang, National Chiao Tung University, Hsing Chu City, Taiwan.

In this paper, a CMOS focal-plane shear sensor is designed and implemented. The adopted motion computation method is based on correlation-based algorithms with modification to detect the local motion vectors whereas the adopted retinal processing circuit is to sense and preprocess the incident image. The proposed shear sensor has a shear-motion-like structure to be selective to the direction and velocity of the images. There are totally 76 pixels, which form four shear-motion detection pairs. The area of a single pixel is $52.96 \times 55.07 \text{ um}^2$ with a fill factor of 16% whereas the chip area is $1151 \times 1116 \text{ um}^2$.

MC2.2

MORTON (Z) SCAN BASED REAL-TIME VARIABLE RESOLUTION CMOS

IMAGE SENSOR, * **O. Yadid-, *E. Artyomov, *Y. Rivenson, **G. Levi, Ben-Gurion University, Beer-Sheva, Israel**, ** University of Calgary, Alberta, Canada.

An image sensor architecture with an alternative image scan method, based on Morton (Z) order, is presented. This scan, compared to the conventional row (raster) scan, enables faster and efficient mean (average) computation of square image blocks. Digital averaging is used and the pixel data is read out with either the original resolution, a 2x2 or a 4x4 block averaging. A test chip of 128×128 array has been implemented in $0.35 \text{ }\mu\text{m}$ CMOS technology, has 15% fill factor, is operated by a 3.3V supply and dissipates 30mW at video rate.

MC2.3

LOW POWER GLOBAL SHUTTER CMOS ACTIVE PIXEL IMAGE SENSOR

WITH ULTRA-HIGH DYNAMIC RANGE, *A. Fish, *A. Belenky, *, **O. Yadid-Pecht, VLSI System Center Ben-Gurion University, Beer-Sheva, Israel, ** University of Calgary, Alberta, Canada.

A novel low power global shutter CMOS Active Pixel Sensor (APS) with ultra-high dynamic range is presented. Incorporating a sample-and-hold element in each pixel, the sensor enables imaging of fast moving objects in the field of view. An adaptive exposure time is automatically applied to each pixel, according to the local illumination intensity level, significantly increasing the dynamic range of the sensor. Driven by low-power dissipation requirements, the proposed pixel is operated by low voltage supply (1.8V). System architecture and operation are discussed and simulations results in a standard 0.35 μ m CMOS technology are presented.

MC2.4

CMOS APS PHOTORESPONSE AND CROSSTALK OPTIMIZATION

ANALYSIS FOR SCALABLE CMOS TECHNOLOGIES, *I. Shcherback, *, **O. Yadid-Pecht, Ben-Gurion University, Beer-Sheva, Israel, University of Calgary, Alberta, Canada.

This work presents an improved semi-analytical model developed for photoresponse estimation of a photodiode based CMOS Active Pixel Sensor (APS). We show its use for maximum pixel photosignal prediction and CMOS APS crosstalk (CTK) optimization. Our model reveals the photosignal and the CTK dependence on the pixel geometrical shape and the pixels arrangement within the array. It brings out clearly the possibility of a design enabling maximum response and/or minimum CTK. It can be used, therefore, as a predictive tool for design optimization.

MC2.5

CMOS SOI IMAGE SENSOR, I. Brouk, Y. Nemirovsky, Technion, Haifa, Israel

Design, operation and measurement results of CMOS camera implemented within SOI wafer are presented. Peak of photodiode quantum efficiency is obtained for the wavelengths of 400-500 nm. In addition, noise measurements of the 1/f noise in p-mos and n-mos transistors for analog applications are reported under wide bias conditions ranging from subthreshold to saturation. Two implementations (in regular and SOI wafers) of 0.35 μ m CMOS analog process are compared and it is found that they exhibit similar 1/f noise. The results of this study are useful to the design and modeling of 1/f noise of CMOS analog circuits.

MD2: SPECIAL SESSION - NEUROMORPHIC SYSTEMS

Monday, December 13

Time: 14:00 – 15:40

Hall: Arbel

Chair: **J. G. Harris**, University of Florida, FL, USA.

MD2.1

TOWARDS A SPIKING VLSI IMPLEMENTATION OF FREEMAN'S

OLFACTORY MODEL, T. A. Holz, J. Harris, University of Florida, Gainesville, FL, USA.

We introduce the Freeman model—a nonlinear dynamical system proposed to model the operation of the cortex—and explain how its interconnected nature complicates physical realizations. We propose changing the Freeman model so that it is a spiking network in order to alleviate the implementation problems while preserving the important dynamic characteristics. We include simulation results showing that our modified spiking model demonstrates those dynamics. Finally, we show experimental results from a VLSI chip implementation of the spiking model as a proof-of-concept.

MD2.2

A WINNER-TAKE-ALL NETWORK WITH SPIKING INPUTS, *M. Oster, *S.

C. Liu, **J. Harris *Institute of Neuroinformatics, Zurich, Switzerland,
**University of Florida, USA.

We present results from an analog VLSI implementation of a winner-take-all network that receives spike trains as input. The connectivity in the network can be configured so that the winner is selected after only two input spikes to the winning neuron. We use bursts of spikes to compensate for the intrinsic mismatch in the input transistors of the neurons. The chip with a network of 64 neurons can reliably detect the winning neuron, that is the neuron that receives spikes with the shortest interspike interval.

MD2.3

SPATIAL ACUITY MODULATION OF AN ADDRESS-EVENT IMAGER, *R. J.

Vogelstein, *U. Mallik, *E. Culurciello, *R. Etienne-Cummings, *G.

Cauwenberghs, **J. Harris, Johns Hopkins University, Baltimore, MD, USA,
**UF, Florida, USA.

We have implemented a foveated vision system that uses an 80 μm address-event neuromorphic image sensor and varies its effective spatial acuity throughout the visual field to use bandwidth more efficiently. Low resolution pixels are created by pooling spikes from neighboring

photoreceptors using overlapping Gaussian kernels. The pooling is effected by routing address-events through a memory-based projective field mapping, and new pixels are created by summing inputs on an array of integrate-and-fire neurons. The fovea can be relocated without physically moving the imager by performing a simple computation in the address domain. We provide an example of the system in operation and compute a figure of merit to quantify foveation savings.

MD2.4

IMPROVED ON/OFF TEMPORALY DIFFERENTIATING ADDRESS-EVENT IMAGER, P. Lichtsteiner, T. Delbruck, J. Kramer, Institute of Neuroinformatics, ETH/University Zurich, Zurich, Switzerland.

We fabricated an improved version of Kramer's ON/OFF transient detecting address event imager reported in ISCAS 2002. The new imager functions over 5 decades of background illumination and has much more symmetrical ON and OFF responses. This imager achieves massive redundancy reduction by temporally differentiating the image contrast.

MD2.5

ACTIVE PIXEL SENSOR WITH ON-CHIP NORMAL FLOW COMPUTATION ON THE

READ OUT, V. Gruev, R. Etienne-Cummings, Johns Hopkins University, Baltimore, MD, USA.

A 250 x 250 Active Pixel Sensor (APS) with on-chip spatiotemporal difference computation capabilities is presented. The spatiotemporal difference imager, fabricated in TSMC 0.35 μ m process, contains in-pixel storage elements for previous and current frames and difference computational units outside the imaging array. A novel scan out technique allows for parallel computation of spatial and temporal 1-D derivatives on read out. The final motion estimation, i.e. the ratio of the temporal and spatial derivatives, is computed off chip, but it can be easily implemented in hardware. Experimental data is presented to validate the accuracy of the magnitude and angle of the computed target velocities. The chip consumes 20mW at 50 fps from 3.3V power supply.

MA3: ANALOG FILTERS

Monday, December 13

Time: 16:00 – 17:40

Hall: Galil

Chair: G. S. **Moschytz**, Bar-Ilan University, Israel.

MA3.1

DYNAMIC RANGE, NOISE AND LINEARITY OPTIMIZATION OF CONTINUOUS-TIME OTA-C FILTERS, *S. Koziel, **A. Ramachandran, *S. Szczepanski, **E. Sanchez-Sinencio, Gdansk *University of Technology, Gdansk, Poland, **Texas A&M University, College Station, TX, USA.

A general framework for performance optimization of continuous-time OTA-C filters is presented. Efficient procedures for evaluating nonlinear distortion and noise valid for any filter of arbitrary order are developed based on matrix description of a general OTA-C filter model. A systematic optimization procedure using equivalence transformations is discussed. An application example of the proposed approach to optimal block sequencing and gain distribution of 8th order cascade Butterworth filter is given. Theoretical results are verified using transistor-level simulation with CADENCE.

MA3.2

NOISE ANALYSIS AND OPTIMIZATION OF CONTINUOUS-TIME ACTIVE-RC FILTERS, S. Koziel, Gdansk University of Technology, Gdansk, Poland.

Noise analysis of continuous-time Active-RC filters is presented based on a general model of integrator-based Active-RC filter, which is analyzed using matrix description. A compact and explicit procedure for evaluating input/output referred noise spectrum of any filter of this class is derived. The algebraic approach is employed especially for efficient use in computer-aided design and optimization of Active-RC filters. An application example of the proposed approach to noise optimization of 3rd order Chebyshev filter is given.

MA3.3

GENERAL ACTIVE-RC FILTER MODEL FOR COMPUTER-AIDED DESIGN AND OPTIMIZATION, S. Koziel, Gdansk University of Technology, Gdansk, Poland.

In the paper, a general topology of continuous-time Active-RC filter is presented. The model includes all possible Active-RC filter structures as particular cases and allows us to analyze them using a unified algebraic formalism. This makes it suitable for use in computer-aided analysis and

design of Active-RC filters. By its construction, the model takes into account finite DC gain and finite bandwidth as well as non-zero output resistance of operational amplifiers. A few examples of application of the presented model to analysis of Active-RC filters are given and potential applications for filter optimization are discussed.

MA3.4

A NOVEL METHOD FOR THE CLOSED-FORM ANALYSIS AND DESIGN OF A 4THORDER SINGLE-AMPLIFIER FILTER, *D. Jurisic, N. Mijat, **G. S. Moschytz, *University of Zagreb, Zagreb, Croatia, **Institute of Technology, Zurich, Switzerland, **Bar-Ilan University, Ramat-Gan, Israel.

In this paper we present a new analytical design procedure for arbitrary-order, single-amplifier class-4 active-RC allpole filters. It is already known that only 2nd- and 3rd-order filters can be designed analytically using classical design methods [1] and the equations of higher order still defy a closed-form solution. The new design method parses the ladder network into consecutive L-sections, and makes use of their subsequent transfer functions that can be calculated iteratively. This will be demonstrated in an example of the closed-form analysis and design of a special case of a 4th-order unity-gain LP filter. The Butterworth and Chebyshev approximations with pass-band ripple 0.1-0.2[dB] are considered. The resulting expressions provide insight into the feasibility of realizing a 4th-order filter. The procedure used for the analysis is mainly not only of academic interest, but may have practical significance for special problems.

MA3.5

ANALYSIS OF LINEAR SYSTEM RESPONSE TO WIDE BAND SIGNALS WITH APPLICATIONS TO FILTERS, A. Yahalom, Y. Pinhasi, The College of Judea and Samaria, Ariel, Israel.

The growing demand for broadband wireless communication links and the lack of wide frequency bands within the conventional spectrum causes us to seek bandwidth in the higher microwave and millimeter-wave spectrum at Extremely High Frequencies (EHF) above 30GHz. One of the principal challenges in realizing modern wireless communication links in the EHF band are phenomena occurring during electromagnetic wave propagation through the atmosphere and in the linear systems of the receiver. A space-frequency approach for analyzing wireless communication channels operating in the EHF band is presented. The signal analysis is studied in the frequency domain, enabling consideration of ultra wide band modulated signals. The theory is employed for the analysis of a communication channel operating at EHF that utilizes pulse amplitude modulated signals.

MB3: SIGMA-DELTA MODULATORS

Monday, December 13

Time: 16:00 – 17:40

Hall: Carmel

Chair: **R. Holzer**, AD, Herzelia, Israel.

MB3.1

AN IF INPUT CONTINUOUS-TIME SIGMA-DELTA ANALOG-DIGITAL CONVERTER WITH HIGH IMAGE REJECTION, J. Shen, K. Pun, C. Choy, C. Chan, The Chinese University of Hong Kong, Hong Kong.

A novel resistor time-sharing technique is proposed to achieve higher image rejection (IR) in the design of an intermediate frequency (IF) continuous time (CT) sigma delta ($\Sigma\Delta$) modulator with integrated IF mixers. A third order CT $\Sigma\Delta$ modulator with current feedforward compensation is designed, as well as current input comparator, digital tunable clock tree, etc. It is also found that, for the first stage of a modulator, the gain of input signal and feedback signal can be scaled down to relieve the harsh requirement of active components input/output swing. This design is implemented in a 0.35 μ m double-poly four metal layers CMOS technology. Active area is 0.4mm² and consumes 14.8mW from a 3.3V power supply. Postlayout simulation with 25MHz IF shows no image signal is present for 4096 output data.

MB3.2

A NOVEL SIGNAL-PREDICTING MULTIBIT DELTA-SIGMA MODULATOR, X. Lu, Concordia University, Montreal, Quebec, Canada.

In this paper, the signal-predicting oversampling scheme is developed for the design of the internal quantizers of multibit delta-sigma modulators. By applying the scheme, it has been derived that, regardless of the resolution of the internal quantizer, only 4 comparators are required in a first-order multibit delta-sigma modulator provided that an appropriate oversampling ratio is chosen. To verify the derived results, an illustrative signal-predicting first-order 4-bit DS modulator with 4 comparators is presented. Simulation results show that the modulator functions very well and when compared with a corresponding modulator with a normal flash internal quantizer, in which 16 comparators have to be used, the proposed modulator demonstrates the advantages of reduced power consumption and silicon area.

MB3.3

A JITTER INSENSITIVE CONTINUOUS-TIME SIGMA-DELTA MODULATOR USING TRANSMISSION LINES, *L. Hernandez, **R. Pieter, *E. Prefasi, *S.

Paton, *M. Garcia, *C. Lopez, *Universidad Carlos III de Madrid, Madrid, Spain, **Ghent University, Gent, Belgium.

This work presents a prototype low pass continuous time sigma delta modulator which uses transmission lines in its loop filter rather than capacitive integrators. As has been shown in prior theoretical work, such a structure allows to desensitize the modulator against clock jitter and excess loop delay. The prototype single-bit modulator was designed for an oversampling ratio of 128. Clocked at 53.7 MHz it achieves a peak SNR of 67 dB. In an experiment with an excessive clock jitter of 1% of the clock period, the SNDR is degraded by only 5dB compared to the case without jitter. This is 15dB better than an equivalent modulator with capacitive integrators.

MB3.4

A 250 MHZ DELTA-SIGMA MODULATOR FOR LOW COST

ULTRASOUND/SONAR BEAMFORMING APPLICATIONS, B. Shem-Tov, M. Kozak, E. G. Friedman, University of Rochester, Rochester, NY, USA.

Single-bit Delta-Sigma modulation reduces the complexity of receive beamformers in ultrasound and sonar imaging applications. These applications, however, require a sampling rate in excess of 220 MHz due to the high bandwidth of the echo signals. In this paper, the design and implementation of a 250 MHz second-order single-bit modulator suitable for ultrasound/sonar applications is presented. The circuit is realized in a 0.18 μm P-well CMOS technology and dissipates 20 mW average power when clocked at 250 MHz. The area of the circuit is 0.24 mm². Post-layout simulations show that the modulator achieves 48 dB maximum SNR and 50 dB dynamic range for a 5 MHz input signal bandwidth.

MB3.5

MULTIBIT DELTA-SIGMA CMOS DAC EMPLOYING ENHANCED NOISE-SHAPED DEM ARCHITECTURE

, *D. Akselrod, **S. Greenberg, **S. Hava, *Motorola, Herzlia, Israel, **Ben-Gurion University, Beer-Sheva, Israel.

A multibit Delta-Sigma (DS) DAC employing enhanced noise-shaped Dynamic Element Matching (DEM) architecture is presented. The architecture for implementing a noise-shaped DEM algorithm for use in multibit Delta-Sigma converters is analyzed. The suggested architecture shows the performance improvement as compared to previous solutions. System operation is discussed and hardware realization of the proposed architecture is described. A five-level DS Digital-to-Analog (D/A) converter incorporating the proposed DEM architecture has been fabricated in a 0.12- μm single-poly CMOS process. Finally, measured results are presented.

MC3: HIGH PERFORMANCE INTEGRATED CIRCUITS

Monday, December 13

Time: 16:00 – 17:40

Hall: Tabor

Chair: **D. Allstot**, University of Washington, Seattle, USA.

MC3.1

IMPEDANCE CHARACTERISTICS OF DECOUPLING CAPACITORS IN

MULTI-POWER DISTRIBUTION SYSTEMS, M. Popovich, E. G. Friedman, University of Rochester, Rochester, NY, USA

To decrease power consumption without affecting circuit speed, several power supply voltages are used in modern high performance ICs such as microprocessors. To maintain the impedance of a power distribution system below a specified level, multiple decoupling capacitors are placed at different levels of the power grid hierarchy. The system of decoupling capacitors used in power distribution systems with multiple power supplies is the focus of this paper. The dependence of the impedance on the power distribution system parameters is investigated. Design techniques to cancel and shift the antiresonant spikes out of range of the operating frequencies are presented.

MC3.2

LOW ENERGY ASYNCHRONOUS ADDERS, I. Obridko, R. Ginosar, Technion, Haifa, Israel

Asynchronous circuits are often presented as a means to achieve low power operation. We investigate their suitability for low-energy applications, where long battery life and delay tolerance is the principal design goal, and where performance is not a critical requirement. Three adder circuits are studied - two dynamic and one based on pass-transistor logic. All adders combine dual-rail and bundled-data circuits. The circuits are simulated at a wide supply-voltage range, down to their minimal operating point. Leakage energy (at 0.18 μ m) is found negligible. Transistor count is found to be an unreliable predictor of energy dissipation. Keepers in dynamic logic are eliminated when possible. A modified version of a two-bit dynamic adder (originally proposed by Chong) is found to dissipate the least amount of energy.

MC3.3

TRAVELLING WAVE LINBO₃ ELECTRO-OPTIC MODULATOR WITH QUASI-PHASE-MATCH CPW STRUCTURE FOR TIME-DOMAIN APPLICATIONS,

O. V. Kolokoltsev, S. V. Koshevaya, R. A. Correa, J. S. Alatorre, M. A. Basurto-Pensado, V. V. Grimalsky, National Autonomous University of Mexico, CD Universitaria, Mexico, Autonomous State University

of Morelos, Cuernavaca Mor., Mexico, ** National Institute for Astrophysics, Optics, and Electronics (INAOE), Puebla, Mexico

A new quasi-phase-match CPW structure used for broadening the optical response of travelling-wave electro-optic Z-cut LiNbO₃ modulators is presented. A non-periodic spatial code of CPW with phase-reversal electrode sections was obtained and optimized by a Genetic Algorithm to provide distortion-less temporal response of the modulator at a Pico second range.

MC3.4

NOISE CHARACTERIZATION OF THE 0.35UM CMOS ANALOG PROCESS IMPLEMENTED IN REGULATED AND SOI WAFERS, I. Brouk,

Y. Nemirovsky, Technion, Haifa, Israel

Noise measurements of the $1/f$ noise in p-mos and n-mos transistors for analog applications are reported under wide bias conditions ranging from subthreshold to saturation. Two implementations (in "regular" and SOI wafers) of 0.35um CMOS process are compared and it is found that they exhibit similar $1/f$ noise. The results of above mentioned characterization of 0.35um process are compared with the similar characterization results of 0.5um CMOS process. The results of this study are useful to the design and modeling of $1/f$ noise of CMOS analog circuits.

MC3.5

A 0.8V CMOS TSPC ADIABATIC DCVS LOGIC CIRCUIT WITH THE BOOTSTRAP TECHNIQUE FOR LOW-POWER VLSI, H. P. Chen, J. B. Kuo,

National Taiwan University, Taipei, Taiwan

This paper reports a novel 0.8V CMOS true-single-phase-clocking (TSPC) adiabatic differential cascode voltage switch (DCVS) logic circuit with the bootstrap technique for low-power VLSI. Via the pass transistors and compensating transistors, TSPC scheme has been obtained for easy clocking. Using the capacitance coupling from the bootstrap transistors, this 0.8V TSPC adiabatic DCVS logic circuit with the bootstrap technique consumes 31% less energy as compared to the one using the clocked adiabatic latch (CAL) approach.

MD3: NEURAL NETWORKS

Monday, December 13

Time: 16:00 – 17:40

Hall: Arbel

Chair: **A. Baric**, University of Zagreb, Croatia / **D. Foty**, Gilgamesh Associates, Fletcher, VT, USA.

MD3.1

SECURITY OF NEURAL CRYPTOGRAPHY, *R. Mislovaty, *E. Klein, *I. Kanter, **W. Kinzel, *Bar-Ilan University, Ramat-Gan, Israel, **Wurzburg University, Wurzburg, Germany.

In this paper we analyze the security of Neural Cryptography, a novel key-exchange protocol based on synchronization of Neural Networks. Various attacks on this protocol were suggested by Shamir et al., and the protocol was shown to be secure against them. A new attack strategy involving a large number of cooperating attackers, that succeeds to reveal the encryption key was recently found.

MD3.2

TEXTURE BOUNDARY DETECTION BASED ON MULTIPLE AND PARALLEL CELLULAR NEURAL NETWORKS, C. H. Huang, C. T. Lin, National Chiao-Tung University, Hsin - Chu, Taiwan.

In this paper, a texture boundary detection model has been introduced. It is inspired by the architecture of retina — the film of human's eyes. Based on the innovation — a multiple and parallel CNN processors, we implemented a retina-like model and thus the boundary of texture can be obtained.

MD3.3

NEW CONDITIONS FOR EXPONENTIAL STABILITY OF DELAY IMPULSIVE NEURAL NETWORKS, Z. Yang, D. Xu, J. Deng, J. Niu, Sichuan University, Chengdu, Sichuan, China.

Impulsive effects, which widely exist in various dynamical systems including neural networks, can influence dynamical behaviors of the systems just as delayed effects. In this paper a generalized model of neural networks involving variable delays and impulses is formulated. By introducing differential inequality with impulsive initial conditions and employing the properties of M-matrix, we obtain new sufficient conditions ensuring global exponential stability of the impulsive delayed system. The results extend and improve the earlier

publications. The example and simulation are given for illustration of the theoretical results.

MD3.4

GLOBAL EXPONENTIAL STABILITY OF COHEN-GROSSBERG NEURAL NETWORKS WITH MULTIPLE TIME-VARYING DELAYS, J. Deng, D. Xu, Z. Yang, Mathematics College, Sichuan University, Chengdu, China.

Exponential stability of the Cohen-Grossberg neural networks with multiple time-varying delays are analyzed. Sufficient conditions for the existence and exponential stability of an equilibrium of the networks are obtained. These conditions are less restrictive than previously known criteria and can be easily verified.

MD3.5

HIGH SPEED AND HIGH RESOLUTION CURRENT LOSER-TAKE-ALL CIRCUIT OF $O(N)$ COMPLEXITY, *A. Fish, *V. Mirlud, *, **O. Yadid-Pecht, Ben-Gurion University, Beer-Sheva, Israel, University of Calgary, Alberta, Canada

A CMOS high performance current mode loser-take-all (LTA) circuit is presented. Based on input currents average computation method, the circuit employs inhibitory and excitatory feedbacks, achieving both high speed and high resolution. The proposed circuit is suitable for operation in a wide variety of applications, such as self organizing neural networks, fuzzy systems and it also can be used to compute the global minimum of the input array. While having very simple structure, the proposed LTA has an $O(N)$ complexity and is easy for implementation. The circuit having 8 cells was designed and simulated in a standard 0.35 μ m CMOS process available through MOSIS, is operated via a 1.8V supply and dissipates 58 μ W of power per cell. Its operation is discussed and simulation results are reported.

TA1: SPECIAL SESSION - GRAND CHALLENGES IN CIRCUITS AND SYSTEMS

Tuesday, December 14

Time: 9:00 – 10:45

Halls: **Galil, Carmel, Tabor, Arbel**

Chair: **J. G. Harris**, University of Florida, Gainesville, FL, USA.

Hall: Galil

TA1.1

CHALLENGES IN ULTRA DEEP SUBMICROMETER HIGH

PERFORMANCE VLSI CIRCUITS, E. G. Friedman, University of Rochester, Rochester, NY, USA.

Fundamental trends specific to high speed, high complexity systems are reviewed, emphasizing many of the primary issues that constrain existing and future digital and mixed-signal integrated systems. These issues are discussed in terms of the evolving criteria that affect each aspect of the VLSI design and synthesis process.

Attention is placed on distinguishing between local vs. global issues. Topics such as dual Vt CMOS circuits and on-chip interconnect noise, determined by the local nature of the circuit structures, are compared and contrasted with larger issues that focus on the global nature of VLSI-based systems such as synchronization styles and clock and power distribution networks.

Hall: Carmel

TA1.2

GRAND CHALLENGES IN IMAGE PROCESSING AND ANALYSIS,

A. Bruckstein, Technion, Haifa, Israel.

The field of image processing and analysis is very broad, encompassing a wide variety of research issues, from efficient encoding of images and video sequences, through image enhancement and restoration to image segmentation, recovering spatial shape from shading and pattern distortions, learning about 3D from multiple unregistered 2D images, of image sequences, and high level image understanding topics. Consequently, researchers in this field rely on an amazingly wide variety of mathematical and computational techniques in their attempts to solve the many problems that arise. The grand challenges in image processing are therefore issues concerning syntheses and synergies between the variety of methods, however, the most important challenge remains the wise choice of problems worth focusing on.

Hall: Tabor

TA1.3

CHALLENGES IN CMOS IMAGER DESIGN, O. Yadid-Pecht, VLSI System Center, Ben-Gurion University, Beer-Sheva, Israel, University of Calgary, Alberta, Canada.

In the last decade, Active Pixel Sensors (APS), which are fabricated in a commonly used CMOS process, enabled the design of image sensors with integrated “intelligence.” Current state of the art CMOS imagers allow integration of all functions required for timing, exposure control, color processing, image enhancement, image compression and ADC on the same die. Moreover, systems with wide dynamic range, motion detection and non-standard readout can be designed. CMOS imagers also offer significant advantages in terms of low-power, low-voltage and monolithic integration, rivaling traditional Charge Coupled Devices (CCD).

This talk will cover state of the art CMOS imager systems and design challenges with the advanced CMOS technologies available. Specifically, ways to improve power consumption in such “smart” sensors, required to cope with the current demand for portable systems are reviewed. In addition, pixel optimization is revisited as more advanced processes are used and pixel pitch is reduced.

Hall: Arbel

TA1.4

GRAND CHALLENGES IN SPATIAL-TEMPORAL COMPUTING ON IMAGE FLOWS, T. Roska, Hungarian Academy of Sciences and the Pazmany P. Catholic University, Budapest, Hungary

One of the most difficult tasks, since the invention of the Computer, has been the solution of nonlinear wave equations. Now, the broader problem is to make a computer operating on Image flows as data and having elementary instructions as solving nonlinear wave equations. Interestingly, almost all of the living sensory systems have similar anatomies and physiology models. The Cellular Wave Computer is exactly doing this. Their implementation is presently mostly 2D. A major challenge how to make it in 3D, and how to make it in nanoscale or by using non-electronic materials. These could lead a new understanding of complexity of computing, as well.

Demonstrations will highlight the latest applications.

TA2: CONVERSION CIRCUITS

Tuesday, December 14

Time: 11:00 – 12:40

Hall: Galil

Chair: **T. Galambos**, Intel, Haifa, Israel

TA2.1

HARDWARE-EFFICIENT PRBGS BASED ON 1-D PIECEWISE LINEAR CHAOTIC MAPS, T. Addabbo, M. Alioto, S. Bernardi, A. Fort, S. Rocchi, V.

Vignoli, University of Siena, Siena, Italy.

In this paper, two families of digital maps derived from the Sawtooth map and from the Tent map are analyzed in terms of suitability for pseudo-random bit generation. In particular, several solutions are investigated taking into account the numerical errors due to the approximation strategy used (truncation/rounding off). To evaluate the performance of the obtained pseudo-random sources a number of statistical parameters and tests that properly measure the characteristics of output bit sequences are considered. Results show that, under specific design conditions, the discretized Sawtooth and Tent maps are suitable for generating long-period bit sequences with an adequate randomness quality.

TA2.2

AN AVERAGE LOW OFFSET COMPARATOR FOR 1.25 GSAMPLE/S ADC IN 0.18UM CMOS, N. Stefano, S. Sonkusale, Texas A&M University, College

Station, TX, USA.

High speed comparators designed using small input transistors exhibit large offsets that affect the dynamic performance of the A/D converter. In this paper, a chopped comparator design is illustrated that uses minimum size input transistors to enable speeds up to 1.25Gsample/s in a TSMC 0.18um CMOS process. Chopping at the inputs of the comparator randomizes its offsets yielding a close-to-zero average offset with only increased white-noise floor. This contributes to the increased dynamic range performance and higher spectral purity at the output of the A/D converter. Chopping is made possible by the use of a new low power, low-cost true binary random number generator instead of the traditional pseudo-random number generators. Power consumption and area are reduced because of relaxed design requirements for the same linearity. The circuit-level simulation results, for a 1V peak to peak input signal, demonstrate superior performance.

TA2.3

A 4GSPS, 2-4GHZ INPUT BANDWIDTH, 3-BITS FLASH A/D CONVERTER, C. Recoquillon, J. B. Begueret, Y. Deval, G. Montignac, A. Baudry, University of Bordeaux, Bordeaux, France.

This paper presents the digitizer developed for the astronomical ALMA project. This ASIC is a monolithic A/D converter implemented in a BiCMOS 0.25 μm SiGe process from STMicroelectronics. The main features of the ADC are a 3 bits resolution (8 quantization levels), an input bandwidth from 2 to 4 GHz with 4 GHz sample rate. The design architecture of this digitizer is based on a conventional flash analog to digital converter structure.

TA2.4

A 10-B 500MSPS CURRENT-STEERING CMOS D/A CONVERTER WITH A SELFCALIBRATED CURRENT BIASING TECHNIQUE, M. Song, S. Hwang, University of Dongguk, Seoul, Korea.

A 10-b 500MSPS current-steering CMOS Digital-to-Analog Converter with internal termination resistors is presented. In order to improve the device-mismatching problem of internal termination resistors, a self-calibrated current bias circuit is designed. With the self-calibrated current bias circuit, the gain error of the output voltage swing is reduced within 0.5%. For the purpose of reducing glitch noises, further, a novel current switch based on a deglitching circuit is proposed. A 10-bit CMOS DAC has been fabricated with a 3V 0.35 μm technology, and it consumes 45mW. The measured SFDR is about 65dB, when an input signal is about 8MHz at 500MHz clock frequency.

TA2.5

SIGNAL PROCESSING BUILDING BLOCKS FOR PIPELINED A/D CONVERTER, R. Suszynski, K. Wawryn, B. Strzeszewski, Technical University of Koszalin, Koszalin, Poland.

This paper presents a high speed and a high resolution pipelined a/d converter relying on a current mode technique. The a/d converter structure is composed of current mode building blocks. All building blocks have been designed, then manufactured in CMOS ams 0.8 μm technology and measured to verify proposed concept.

TB2: VIDEO AND MULTIMEDIA TECHNOLOGY

Tuesday, December 14

Time: 11:00 – 12:40

Hall: Carmel

Chair: **S. Greenberg**, Freescale Semiconductor, Beer-Sheva, Israel

TB2.1

MULTISTAGE QUANTIZATION VIA CONDITIONAL HIERARCHICAL MAPPING, A. Eshet, M. Feder, Tel-Aviv University, Tel-Aviv, Israel.

Progressive representation can be realized via a set of quantizers, where the quantizers correspond to an increasing level of refinement. This is referred to as multistage quantization. The work presented in the paper provides an extension to embedded multistage scalar quantization. It allows progressive coding with any set of scalar quantizers, where the partitions are not necessarily embedded, using an efficient, novel multi-layer mapping scheme. It is applicable for progressive coding of raw image and video data and for progressive extension to compression schemes like JPEG and MPEG.

TB2.2

RING-SHAPED N+/P -WELL PHOTODIODE: STUDY OF RESPONSIVITY ENHANCEMENT, *T. Danov, *I. Shcherback, *, **O. Yadid-Pecht, Ben-Gurion University, Beer-Sheva, Israel, University of Calgary, Alberta, Canada.

In this work the possibilities of CMOS APS spectral response improvement is discussed. Thorough submicron scanning results obtained from various ring-shaped pixel photodiodes with different inner radius, implemented in a standard CMOS 0.35 μ m technology, are compared with numerical computer simulations. The functional dependence of the pixel response on the ring opening size was discovered and formulated for various wavelengths illumination. We show that the photodiodes with small ring-opening exhibit better sensitivity in the blue spectrum range (420-460 nm). Comparison between the simulation and measurement results shows a good agreement and, therefore, involving specific photodiode enables to improve the pixel color selectivity design.

TB2.3

A HIGH PRECISION AND LOW NOISE S/H CIRCUIT DESIGN FOR VIDEO SIGNAL SAMPLING, *D. Xu, **X. Lai, **L. Hu, **H. Wang, *University of Teesside, Middlesbrough, UK, **Xidian University, Xian, China.

This paper presents an improved Sample/Hold (S/H) circuit design for analog LCD applications. The circuit possesses the dual characteristics of high

sampling precision and low switch noise and is, thus, suitable for video signal sampling applications. In order to increase accuracy of sampling and to reduce switch noise, the design uses an operational amplifier with current-mode switch, which incorporates an improved buffer amplifier, and introduces a noise elimination technique by using differential amplifier. The simulation results show that for a typical signal sampling application and its Bi-CMOS implementation, the design has achieved a minimal signal distortion and significantly reduced noise effect.

TB2.4

STENCIL SHADOW VOLUMES FOR COMPLEX AND DEFORMABLE OBJECTS, Z. Mihajlovic, I. Kolic, L. Budin, University of Zagreb, Zagreb, Croatia.

We present real-time shadow method based on the shadow volume that exploit capabilities of the modern graphics cards. Algorithm is primarily created for casting shadows of a highly concave complex objects such as trees. For those objects silhouette calculation that is usually preformed by other shadow volume algorithms is complicated and poorly justified. Instead of calculations, it is better to assume a worst case scenario and use all of the edges for construction of the shadow volume mesh, skipping silhouette determination entirely. The achieved benefit is that all procedure, the object and shadow calculation and rendering, could be done on GPU. Proposed solution for shadow casting allows open edges. Indexed vertex blending is used for shadow projections, and the only calculation required is determining projection matrices. Once created, shadow volume is treated like any other mesh.

TB2.5

ALGORITHM FOR FACIAL WEIGHT-CHANGE, U. Danino, N. Kiryati, M. Furst, Tel- Aviv University, Tel-Aviv, Israel.

A facial weight-change simulator is presented. It is intended for use in the evaluation of self-perception distortion of Anorexia Nervosa (AN) patients. Processing begins with the extraction of the face from the background. Using minimal user intervention, the face is then divided into regions characterized by different weight-change patterns. A mathematical transformation that models growth and shape modification in living organisms is applied to each region. Finally, a unified color face image is generated, in which the face appears fatter or thinner as intended.

TC2: PROCESS AND DEVICE SIMULATION

Tuesday, December 14

Time: 11:00 – 12:40

Hall: Tabor

Chair: **G. Robins**, University of Virginia, Charlottesville, VA, USA

TC2.1

EXPERIMENTAL EXTRACTION OF POINT DEFECTS PARAMETERS NEEDED FOR 2-D PROCESS SIMULATION USING REVERSE MODELING,

E. N. Shauly, G. Richard, Y. Komem, Tower Semiconductor, Migdal Ha'Emek, Israel.

This work deals with the simulation of two-dimensional impurity diffusion in CMOS silicon devices. The Reverse Modeling method was used to determine the diffusion coefficient (DI), surface recombination rate of defects (KI) and the characteristics of the injecting source. Analysis showed similarity between DI in 2-D system compared with the value obtained from non-patterned samples. The results for DI and KI are very well described by the Arrhenius expressions. DI was found to be related to the substrate type e.g. EPI or CZ. The values of KI related to the interface type, oxidizing or non-oxidizing (SiO₂ or Si₃N₄).

TC2.2

ANALYSIS AND SIMULATION OF SPIRAL INDUCTOR FABRICATED ON SILICON SUBSTRATE,

S. Yoshitomi, TOSHIBA Corp, Semiconductor Company, Yokohama, Kanagawa, Japan.

The simple but completely physically based modeling methodology for spiral inductor is proposed. This method consists of two steps and solves all the model parameters without using any optimization. Further investigation on the parameter extraction has pointed out clear physical dependencies on the layout parameters and other physical effect has also been observed. Modeling accuracy by using s-parameter and RF-noise figure has been checked and it has proven that this modeling methodology is valid up to 20GHz.

TC2.3

RAPID CAD PROTOTYPING FOR NANOTECHNOLOGY USING

OBJECTIVE-C AND COCOA, A. K. Jones, B. Brady, I. Kourtev, University of Pittsburgh, Pittsburgh, PA, USA.

Future nanotechnologies will permit the manufacturing of computational systems of unprecedented complexity. It is not unreasonable to anticipate that, in order to analyze and design such systems, engineers will rely heavily on Computer-Aided Design (CAD) software tools. As is the case with

semiconductor CAD tools, the better one understands the underlying data structures and algorithms of a CAD tool, the more productive user of the CAD tool one is. The increasing challenges of future nanosystems will likely lead to blurring the division between system designers and the CAD designers and to merging of these two disciplines. Novel software development environments permitting powerful development of high-quality software will be required. This paper describes the experience of the authors with one such development framework based on the Objective-C programming language and the Cocoa application programming environment in a UNIX-based environment. These development choices were made because of the available programmer support, permitting development of complex applications in a straightforward way. A CAD application of moderate complexity for the simulation of asynchronous cellular arrays was developed with minimal effort. The authors believe that the ease of development using Cocoa is greater than in other similar development environments.

TC2.4

DESIGN OF WAVEGUIDING PHOTONIC BANDGAP DEVICES BY USING THE BLOCKFLOQUET THEOREM, A. G. Perri, A. Giorgio, R. Diana, Polytechnic of Bari, Bari, Italy.

The design of some 1-D waveguiding photonic bandgap (PBG) devices has been carried out by a model based on the Bloch-Floquet theorem. A low loss, very narrow passband GaAs PBG filter having an air bridge configuration, was designed and simulated. Moreover, a resonant Si on glass PBG device has been designed.

TC2.5

EVALUATION OF THE NEW OASIS FORMAT FOR LAYOUT FILL COMPRESSION, *G. Robins, **A. Zelikovsky, ***Y. Zheng, *University of Virginia, Charlottesville, VA, USA, **Georgia State University, Atlanta, GA, USA, ***University of California, San-Diego, CA, USA.

We analyze the data compression capability of the new Open Artwork System Interchange Standard (OASIS), the successor to the GDSII format. Our experiments confirm the advantage of OASIS compression over GDSII in the context of layout fill generation, a critical step in VLSI manufacturing. We propose new OASIS-based compression algorithms which outperform industry tools.

TD2: BIOMEDICAL AND INDUSTRIAL APPLICATIONS

Tuesday, December 14

Time: 11:00 – 12:40

Hall: Arbel

Chair: **R. Ginosar**, VLSI Systems Research Center, Technion, Haifa, Israel/ **A. Morgenshtein**, Technion, Haifa, Israel

TD2.1

NEW ISFET CATHETERS ENCAPSULATION TECHNIQUES FOR BRAIN PH IN-VIVO MONITORING, L. Sudakov-Boreysha, U. Dinnar, Y. Nemirovsky, Technion, Haifa, Israel.

This work presents new concepts of ISFET encapsulations for catheters in brain in-vivo monitoring. Plain-chip and flip-chip bonding techniques are introduced. In both techniques pseudo-reference electrode is implemented.

TD2.2

THE ESO-PILL™ TM A NON-INVASIVE MEMS CAPSULE FOR BOLUS TRANSIT MONITORING IN THE ESOPHAGUS, *Y. T. Jui, **D. Sadowski, *K. Kaler, *M. Mintchev, *University of Calgary, Calgary, Alberta, Canada, **University of Alberta, Edmonton, Alberta, Canada.

Monitoring bolus transit in the esophagus has been pivotal for the diagnosis of achalasia, diffuse spasm, motor abnormalities associated with systemic disorders, and gastro-esophageal reflux disease. Despite recent advances in X-Ray imaging and the introduction of multichannel intraluminal impedancometry, these studies remain moderately invasive. Barium radiography subjects the patient to X-Ray radiation, while the new technique of impedance monitoring employs catheters introduced either transnasally or transorally. Rapid developments in microelectronics, micro-electromechanical systems (MEMS) and wireless radio-frequency (RF) transmission created the possibility of suggesting a conceptually different and completely non-invasive technique for esophageal bolus transit testing. In the present study, the concept of the ESO-Pill™ is introduced, a non-invasive swallowable “smart” microelectronic capsule, which can monitor in real time its acceleration, velocity of propagation, position, and the contractile force that pushes it as it passes through the esophagus. The capabilities and the limitations of the ESO-Pill™ are discussed in the context of the radically different type of measurements that such device could offer, while every attempt is made to associate these measurements with the presently available bolus transit monitoring standards in esophageal testing.

TD2.3

MICROLENS ARRAY HELP IMAGING HIDDEN OBJECTS FOR MEDICAL APPLICATIONS, D. Abookasis, J. Rosen, Ben-Gurion University, Beer-Sheva, Israel

We propose and experimentally demonstrate a new method of seeing objects hidden in scattering medium from multiple speckle images. The objects hidden between two biological tissues (chicken breast) are reconstructed from many speckled images formed by a microlens array. Each microlens from the array projects a small different speckle image of the hidden object onto a CCD camera. The entire noisy images from the array are digitally processed to obtain the desired image of the hidden objects. Following the first proposed method, a different algorithm implemented on the same optical system has been developed. This modified algorithm, based on the point-source reference method improves the resolution of the previous method. Laboratory experiments with two kinds of objects are presented.

TD2.4

IMPROVEMENT OF ILLUMINATION ARTIFACTS IN MEDICAL ULTRASOUND IMAGES USING A BIOLOGICALLY BASED ALGORITHM FOR COMPARISON OF WIDE DYNAMIC RANGE, H. Spitzer, Y. Zimmer, Tel-Aviv University, Tel-Aviv, Israel.

Medical ultrasonic B-scans often suffer from inherent artifacts that originate from the attenuation properties of the sonic beam in the living tissues. Common methods such as Time Gain Compensation (TGC) do not yield satisfactory results. We tested a previous algorithm for compression of wide dynamic range in an attempt to address the above problem. This algorithm is based on a biological model that was also suggested for wide dynamic range and lightness constancy. It is based on retinal mechanisms of adaptation (gain control), both 'local', and 'remote', that enable also video image applications by taking into account the dynamics of human adaptation mechanisms. The results indicate that the algorithm succeeded in automatically exposing the details in very bright (i.e., saturated) and very dark zones in the same image. Such an exposure appears as a promising significant tool for better clinical diagnosis.

TA3: POWER ELECTRONICS

Tuesday, December 14

Time: 14:00 – 15:40

Hall: Galil

Chair: **P. Schechner**, Ort B. A. College of Engineering, Carmiel, Israel.

TA3.1

SHUNT VOLTAGE REGULATORS FOR AUTONOMOUS INDUCTION GENERATORS, PART I: PRINCIPLES OF OPERATION, A. Kuperman, R.

Rabinovici, Ben-Gurion University, Beer- Sheva, Israel.

This paper gives the theoretical background of output voltage regulation for autonomous induction generators. Based on the equivalent circuit of an induction generator, conditions for maintaining constant voltage are derived at given reference, rotation speed and load changes. It is shown that by adjusting the reactive power source connected to the induction generator terminals it is possible to maintain the generator output voltage within a given operating range. Limits of such a regulation are also shown and explained. A simple controller scheme is given to enforce the theoretical aspects, with extended simulation results presented.

TA3.2

SHUNT VOLTAGE REGULATORS FOR AUTONOMOUS INDUCTION GENERATORS, PART II: CIRCUITS AND SYSTEMS, A. Kuperman, R.

Rabinovici, Ben-Gurion University, Beer- Sheva, Israel.

This paper presents different kinds of circuits used for autonomous induction generators output voltage regulation. Operation of SVC and STATCON based voltage regulators is explained, advantages and disadvantages of each type are shown. Different control strategies of voltage source and current source inverter based STATCONs are discussed. A novel current sensorless fixed frequency type of voltage regulator is also shown. In addition, extended simulation results are given, based on a real induction machine data.

TA3.3

HIGH-VOLTAGE TOLERANT WATCHDOG COMPARATOR IN A LOW-VOLTAGE CMOS TECHNOLOGY, V. Potanin, E. Potanina, National

Semiconductor Corporation, Santa Clara, CA, USA.

Presented is a watchdog comparator that is tolerant of supply voltages significantly higher than the process limit for individual CMOS transistors. The circuit demonstrates very low current consumption, while fast dynamic response. The described circuit was implemented in a battery charge block of

a power management IC for cellular phones. The implemented watchdog comparator is tolerant of input voltages up to 12 V and passes operational life and reliability tests. Extensive evaluation under various start-up conditions shows circuit compliance to contradictory specification parameters. Simulation and measurement data for various power-up transient conditions are presented.

TA3.4

A RESTRICTION ON THE POWER SYSTEM BY THEORETICAL REQUISITIONS OF THE BCU METHOD, N. Jiang, W. Song, Southeast University, Nanjing, China.

In power system transient stability analysis, boundary of stability region based controlling unstable equilibrium point method (BCU method) has gained much concern due to its sound theoretical foundations. Among requisitions in theory of the bcu method, the one-parameter-transversality condition is difficult or even impossible to check directly. Under these requisitions, it is proved that, if the corresponding lossless system is not complete stable, a gradient system should not be complete stable either. This suggests an indirect approach in verifying the abstract conditions. A sufficient condition for not-complete stability of the gradient system is also proposed.

TA3.5

PERFORMANCE OF A GLUCOSE AFC, *L. Mor, *E. Bubis, **K. Hemmes, *P. Schechner, *Ort Braude Academic College of Engineering, Carmiel, Israel, **Delft University of Technology, Delft, the Netherlands.

Room Temperature measurements performed in an Alkaline Fuel Cell using glucose as fuel at different concentrations are reported. The Open Circuit Voltage as function of initial glucose concentration, Polarization Curves and Power Density as function of Current Density were measured. It was found that the reported electrical properties as function the initial glucose concentration have a maximum value around 0.89 M. This behavior is attributed to second order reactions that compete with the electrochemical oxidation of the glucose.

TB3: MIXED-SIGNAL CIRCUITS

Tuesday, December 14

Time: 14:00 – 15:40

Hall: Carmel

Chair: **I. Wagner**, IBM Haifa Labs, Haifa, Israel / **J. Shappir**, Bar-Ilan University, Ramat-Gan, Israel

TB3.1

A SPIKE-BASED ADAPTIVE FILTER, X. Gong, J. Harris, University of Florida, Gainesville, FL, USA

We propose a spike-based adaptive filter with supervised learning. Unlike standard adaptive filters, here the optimal MSE solution is not unique for the spike-based system identification problem. The simplex method is introduced to select one of the many possible optimal solutions. In simulations, an LMS-based learning procedure is designed and, for faster convergence, we introduce the credit assignment method which penalizes all the weights contributing to the current error signal. Finally, we discuss issues regarding the implementation of the spike based adaptive filter in an analog VLSI circuit.

TB3.2

A ROBUST OFFSET CANCELLATION SCHEME FOR ANALOG MULTIPLIERS, X. Wang, Z. Shi, S. Sonkusale, Texas A&M University, College Station, TX, USA.

A new robust offset cancellation scheme for analog multipliers is presented. The offset signal is extracted from the multiplier output using a digital integrator and is fed back to the input for cancellation. This scheme cancels the offset at both the inputs of analog multipliers. The cancellation circuitry is simple and mostly digital, so is suitable for on-chip implementation. The circuit and a Gilbert multiplier are designed in TSMC0.18um CMOS technology to verify the scheme. Schematic simulation shows that the cancellation can greatly attenuate the DC offset and harmonics.

TB3.3

SPARSE APPROXIMATIONS WITH A HIGH RESOLUTION GREEDY ALGORITHM, B. Salomon, H. Ur, Tel-Aviv University, Tel-Aviv, Israel.

Signal decomposition with an overcomplete dictionary is nonunique. Computation of the best approximation is known to be np-hard problem. The matching pursuit (mp) algorithm is an iterative greedy algorithm that finds a

sub-optimal approximation, by picking at each iteration the vector that best correlates with the present residual. choosing approximation vectors by optimizing a correlation inner product can produce a loss of time and frequency resolution. we propose a modified mp, based on a post processing step applied on the resulting mp approximation, using backward greedy algorithm, to achieve higher resolution than the original mp.

TB3.4

A CPFASK/PSK-PHASE RECONSTRUCTION-RECEIVER FOR ENHANCED DATA RATE BLUETOOTH SYSTEMS, *D. Bruckmann, **M. Hammes, **A. Neubauer, *University of Wuppertal, Wuppertal, Germany, **Infineon Technologies, Dusseldorf, Germany.

A well-established receiver concept for wireless systems is based on a low IF-architecture with a simple limiter used for digitization. This architecture can be applied with negligible performance degradation to simple 2-ary modulation schemes with constant envelope signals like GFSK. In order to achieve higher data rates the wireless standards like Bluetooth are enhanced with additional modes using more sophisticated modulation schemes. With respect to implementation costs and power consumption it is desirable to realize a combined CPFASK/PSK-receiver, which performs digitization by simple comparators or 1-bit A/D-converters also for the higher data rate schemes. In this contribution it will be shown how to achieve the required performance with a simple limiter in the receive path and optimized signal processing before and after quantization.

TB3.5

A LOW COMPLEXITY COORDINATED FEXT CANCELLATION FOR VDSL, A. Leshem, L. Youming, Bar Ilan University, Ramat-Gan, Israel.

In this paper we study a simplified linear precoding scheme for FEXT cancellation in VDSL downstream transmission. We compare the proposed method to ideal zero forcing (ZF) FEXT cancellation and show that for multipair VDSL systems the method achieves rates that are close to the optimal theoretical rates without FEXT. We also derive a simple lower bound on the performance that allows us to predict the performance of the proposed algorithm. We end up with testing the proposed method on theoretical and empirical channels.

TC3: SYSTEM AND DEVICE MODELING

Tuesday, December 14

Time: 14:00 – 15:40

Hall: Tabor

Chair: **G. Robins**, University of Virginia, Charlottesville, VA, USA

TC3.1

SOC MODELING METHODOLOGY FOR ARCHITECTURAL EXPLORATION AND SOFTWARE DEVELOPMENT, M. Silbermintz, A. Sahar, I. Peled, M.

Anschel, E. Watralov, H. Miller, E. Weisberger, Motorola Semiconductor Israel, Herzelia, Israel.

This paper introduces a System On Chip (SOC) modeling methodology that enables the use of a single model for multiple purposes throughout a project's life cycle, starting from the architectural definition phase, continuing with the micro-architectural optimization and ending with the software development and optimization phase. These different purposes are served by enabling multiple approaches for modeling applications, providing capabilities for configuring and refining the hardware model and reaching high accuracy level while maintaining a good simulation speed.

TC3.2

ENHANCEMENT OF THE SEMISYMBOLIC ANALYSIS PRECISION USING THE VARIABLE-LENGTH ARITHMETIC, J. Dobes, J. Michal, Czech

Technical University, Praha, Czech Republic.

An optimal pivoting strategy for the reduction algorithm transforming the general eigenvalue problem to the standard one is presented for both full- and sparse-matrix techniques. The method increases the precision of the semisymbolic analyses especially for large-scale circuits. The accuracy of the algorithms is furthermore increased using longer numerical data. First, a long double precision sparse algorithm is compared with the double precision sparse and full-matrix ones. Further, the application of a suitable multiple-precision arithmetic library is evaluated. Finally, using the longer numerical data to eliminate possible imprecision of the multiple eigenvalues is evaluated.

TC3.3

MODELING OF ANALOG CIRCUITS BY USING SUPPORT VECTOR REGRESSION MACHINES, A. Baric, V. Ceperic, University of Zagreb,

Zagreb, Croatia.

The support vector regression method is used for modeling of electronic circuits. The method ensures simple, robust and accurate modeling of

electronic circuits. It yields very good results for situations not specified in the learning data set, demonstrating very good generalization property of support vector machines. The method is applicable to modeling based on the measurements or device-level circuit simulations. Several GaAs circuits (buffer, resistive mixer, ring oscillator) are modeled using the proposed method.

TC3.4

ANALYSIS OF HARMONIC DISTORTION IN DEEP SUBMICRON CMOS, M. Bucher, A. Bazigos, N. Nastos, Y. Papananos, F. Krummenacher, S. Yoshitomi, Technical University of Crete, Chania, Crete.

This paper presents a study of harmonic distortion measurement and modeling in an 0.14 μ m CMOS technology. Measurements and simulation of DC characteristics, as well as high-frequency harmonic distortion are presented. The new EKV3.0 compact MOSFET model is used to model DC and harmonic distortion characteristics.

TC3.5

A COMPACT METHOD FOR OBTAINING THE HYBRID PARAMETERS OF THE BJT AMPLIFIER, A. M. Al-Smadi, Q. Al-Zobi, Yarmouk University, Irbid, Jordan.

The hybrid equivalent circuit continues to be very popular in the analysis of small-signal ac response of the BJT amplifier. The manufacturers continue to specify the h-parameter for a particular operating region on the specification sheets. However, specification sheets can not provide parameters for an equivalent circuit at every possible operating point. Hence, the parameters defined at an operating point may or may not reflect the actual operating conditions of the amplifier. This paper addresses a method for determining the h-parameter using a single compact graph.

TD3: CONTROL SYSTEMS AND APPLICATIONS

Tuesday, December 14

Time: 14:00 – 15:40

Hall: Arbel

Chair: **Y. Bar-Shlomo**, Ort B. A. College of Engineering, Carmiel, Israel

TD3.1

DISTRIBUTED SYSTEM DESIGN AND CONTROL VIA MULTIPLE OBJECTIVES OPTIMIZATION, *I. Rusnak, **A. Guez, **R. Cochran, *Rafael, Haifa, Israel, **Drexel University, Philadelphia, PA, USA.

An optimization approach to distributed intelligent system design and control is presented. It is expected to enhance the autonomous decision-making capabilities of systems functioning as members of a team. It is applicable to autonomous distributed agents within homogeneous or heterogeneous clusters, when they must collaborate as a team to achieve a common goal. This approach inherently supports situation awareness, collision avoidance, and operations in a complex environment that may experience both degraded communications and sensor failures. An example that demonstrated the approach for large number of agents is presented.

TD3.2

CONTROLLING AN ELECTRICAL MOTION SYSTEM BY A LOAD INSTRUCTION DECODING ALGORITHM USING FPGA, A. Kuperman, S. Cooper, R. Rabinovici, Ben-Gurion University, Beer-Sheva, Israel.

This paper presents a motion control system which employs a load decoder, capable of analyzing the load value and changes, applied to the motor's rotor, decoding them into an instruction set for the controller input. The system is implemented in a Field Programmable Gate Array (FPGA) device, which have recently become affordable for implementing complicated motion control algorithms. All motion control logic is implemented in hardware (no software at all) and executes functions by the dedicated hardware logics. In such case execution time becomes inherently fast and deterministic. This complicates the design, compared to the rather simple solution in software on DSP but offers reduced control system price that is essential for mass production applications. Moreover it can be easily transformed into ASIC for further cost reduction.

TD3.3

NANOROBOTIC CHALLENGES IN BIOMEDICAL APPLICATIONS, DESIGN AND CONTROL, *A. Cavalcanti, ,*L.C. Kretly **L. Rosen, **M. Rosenfeld, **S. Einav, *Unicamp University of Campinas, Campinas, Brazil, **Tel Aviv University, Tel Aviv, Israel.

Ongoing developments in molecular fabrication, computation, sensors and motors will enable the manufacturing of nanorobots - nanoscale biomolecular machine systems. The present work constitutes a novel simulation approach, intended to be a platform for the design and research of nanorobots control. The simulation approach involves a combined and multi-scale view of the scenario. Fluid dynamics numerical simulation is used to construct the nanorobotic environment, and an additional simulation models nanorobot sensing, control and behavior. We discuss some of the most promising possibilities for nanorobotics applications in biomedical problems, paying a special attention to a stenosed coronary artery case.

TD3.4

NUMERICAL ALGORITHM FOR MEASUREMENT OF ANGLE PHASE SHIFT FOR SINES SIGNAL, A. Aksamovic, S. Konjicija, University of Sarajevo, Sarajevo, Bosnia and Herzegovina.

This paper presents one method for measurement of phase shift between signals in electric power system (EPS), such as voltages or currents. The presented algorithm is very simple and efficient, and it can be used for purposes of protection, control and measurement in EPS, as well. The algorithm is based on mathematically simple expressions, which don't require high processing power, so it is convenient for single chip applications. This algorithm is considered with high and low sampling rate, and proper pre-processing of signal in integrated data acquisition and control systems in EPS is proposed. It is shown that the achieved accuracy can satisfy requests of intended application.

TD3.5

A NEW METHOD TO ANALYSE THE UNIQUE STEADY STATE OF NONLINEAR NONAUTONOMOUS CIRCUITS, *F. Ping, **W. Erzhi, ***P. Cooke, *S. Yuanchun, *Logistical Engineering University, Chongqing, China, **Shenyang Polytechnic University, Shenyang, China, ***Adelaide University, North Terrace, South Australia.

A new method to prove the unique steady state of nonlinear nonautonomous circuits by vector comparison is introduced. The main results obtained in this paper show that the unique steady state of nonlinear nonautonomous circuits can be determined by Hurwitz conditions of a constant matrix. The restriction to the elements of the matrix is just that the slope of the constitutive relation is bounded, which is a much looser condition than the demands put forward by previously published papers. The new criteria in this paper have much wider applicability than the results already known.

TA4: ANALOG CIRCUITS AND APPLICATIONS

Tuesday, December 14

Time: 16:00 – 17:40

Hall: Galil

Chair: **T. Galambos**, Intel, Haifa, Israel.

TA4.1

INPUT-FREE CASCODE V_{th}N AND V_{th}P EXTRACTOR CIRCUITS, *Y.

Wang, *G. Tarr, **Y. Wang, *Carleton University, Ottawa, ON, Canada,

**Concordia University, Montreal, Quebec, Canada.

Input-free NMOS and PMOS V_{th} (threshold voltage) extractor circuits using cascode structure to eliminate the error caused by body effect are presented. The extracted V_{th} for NMOS and PMOS is referenced to ground and VDD respectively. Both NMOS and PMOS V_{th} extractor have high accuracy of almost 100% from the Hspice simulation. The NMOS and PMOS extractor circuits have been simulated in Hspice using TSMC 0.35 μ m CMOS technology at 2V and 2.9V power supply with low power consumption of 0.29mW and 0.44mW respectively.

TA4.2

FUZZY DECISION DIAGRAM REALIZATION BY ANALOG CMOS

SUMMING AMPLIFIERS, *I. *Levin, **V. Varshavsky, *V. Marakhovsky, *A.

Ruderman, *N. Kravchenko, * Bar Ilan University, Ramat-Gan, Israel, **The University of Aizu, Aizu-Wakamatsu, Japan.

A functional completeness of summing amplifier with saturation in a multi-valued logic of an arbitrary value proven in previous works gives a theoretical background for analog implementation of fuzzy devices. Practical design techniques for multi-valued analog fuzzy controllers still have to be developed. Compared with the traditional approach, analog CMOS fuzzy controller implementation has the advantages of higher speed, lower power consumption, smaller die area and more. The paper introduces some special design techniques and provides design example for an industrial fuzzy controller implementation solidified by SPICE simulations.

TA4.3

A LOW-POWER ANALOG SPIKE DETECTOR FOR EXTRACELLULAR NEURAL RECORDINGS, C. L. Rogers, J. Harris, University of Florida,

Gainesville, FL, USA.

This paper discusses a low-power spike detection circuit, which reduces bandwidth from neural recordings by only outputting a short pulse at each

neural spike time. Communication bandwidth is dramatically reduced to the number of spikes. The principal idea is to use two low pass filters, one with a higher cutoff frequency to remove high frequency noise and the other with a lower cutoff frequency to create a local average. When the difference between the signal and the local average rises above a threshold a spike is detected. The circuit uses subthreshold CMOS to keep the power consumption low enough for integration of many channels in an implanted device. This spike detection method shows promising results towards a robust and unsupervised algorithm that is lower power and more compact than existing spike detection methods.

TA4.4

A 2.4GHZ FULLY CMOS INTEGRATED RF TRANSCEIVER FOR 802.11B WIRELESS LAN APPLICATION, W. Kong, University of Maryland, College Park, MD, USA.

A fully CMOS integrated RF transceiver for 802.11b wireless LAN application is implemented and measured. The IC is fabricated in 0.25um CMOS process and packaged in TQFP package. The single chip transceiver incorporates an I/Q modulator and demodulator, an integrated IF and RF synthesizer with on-chip VCOs, an on-chip LNA, and PA pre-driver amplifier. The chip fully complies with the IEEE 802.11b WLAN standard. The transmitter achieves less than 7.5% EVM and the receiver sensitivity is -86dBm for 11Mbps mode. The chip uses 3V power supply and the current consumption is 60mA for receiver and 70mA for transmitter.

TA4.5

DESIGN OF A DIFFERENTIAL CHAOTIC COLPITTS OSCILLATOR, *O. Tsakiridis, **E. Zervas, ***D. Syvridis, ***M. Tsilis, *J. Stonham, *Brunel University Uxbridge, Middx, UK, **TEI-Athens, Athens, Greece, ***University of Athens, Athens, Greece.

A differential bipolar Chaotic Colpitts Oscillator is presented. Compared to the classical Colpitts oscillator the Differential Chaos Colpitts Oscillator (DCCO) produces anti-phase dual output chaotic carriers and the circuit is insensitive to any extra parasitic components. Pspice simulations performed up to 1 GHz, demonstrate the effectiveness of DCCO.

TB4: COMMUNICATION RECEIVERS

Tuesday, December 14

Time: 16:00 – 17:40

Hall: Carmel

Chair: **M. A. Lagunas**, CTTC, Barcelona, Spain

TB4.1

FAST ACQUISITION ARCHITECTURES FOR DIRECT-SEQUENCE SPREAD-SPECTRUM SYSTEMS, D. M. Frai, A. Reichman, Tel-Aviv

University, Tel-Aviv, Israel.

This paper presents, a comprehensive coverage of Direct-Sequence Spread-Spectrum fast acquisition techniques and architectures, their performance and complexity. A TDMA/CDMA transmission structure is presented as a burst of direct sequence spread spectrum signal. Fast parallel acquisition architectures are overviewed, examined, and compared in perspective of performance and complexity. New architectures are presented, showing tradeoff between performance and complexity. The architectures evaluation is made from a novel point of view. It is based on the acquisition success probability in a finite time instead of evaluating the traditional . All architectures use parallel processing with sequence matched filters and partial sequence matched filters, and FFT algorithm.

TB4.2

ML ITERATIVE TENTATIVE-DECISION-DIRECTED (ML-ITDD): A CARRIER SYNCHRONIZATION SYSTEM FOR SHORT PACKET TURBO CODED COMMUNICATION, Y. Rahamim, A. Freedman, A. Reichman, Tel-Aviv

University, Tel-Aviv, Israel.

The invention of Turbo Codes has manifested the ability of communications systems to operate at very low signal to noise ratio, very close to the theoretical Shannon capacity limit. However, synchronization of turbo-coded signals operating in low SNR conditions may be difficult, especially for short packet transmission. This paper proposes the Maximum-Likelihood Iterative-Tentative-Decision-Directed (ML-ITDD) circuit for using the tentative decisions produced by the turbo decoder to improve the carrier synchronization in turbo coded short packets communication systems. The ML-ITDD method operates iteratively and jointly with the turbo decoder, enhancing both the turbo-decoder and the synchronization performance. The ML-ITDD method has been shown by simulation to significantly increase the allowed initial frequency and phase uncertainty region, thus allowing the use of very short training sequences for initial carrier synchronization.

TB4.3

TIMING RECOVERY OF PAM SIGNALS USING BAUD RATE

INTERPOLATION, N. Sommer, Texas Instruments, Herzlia, Israel.

The timing recovery function of a digital communications receiver has to set the sampling instants of the analog-to digital (A/D) converter. The natural solution is to modify the clock signal that controls the A/D (e.g. by using a voltage controlled oscillator). However, this is an expensive solution, and it is usually preferred that the A/D will sample with a free-running clock, and timing modifications will be done by digital interpolation of the A/D output samples. Such interpolation is practical only if the sampling rate is high enough such that a data sample can be reconstructed from several neighboring samples. However, fast digital data communications standards (such as Gigabit Ethernet) usually use baud rate sampling (one sample per symbol), which is below the Nyquist rate of the signal, and certainly cannot be used with standard interpolation techniques. This paper suggests to exploit the structure of Pulse Amplitude Modulation (PAM) communications signals in order to perform interpolation at baud-rate sampling. With such interpolation, only a simple and cheap control of the A/D clock is required.

TB4.4

ANALYSIS OF LOCK-LOSS EVENTS IN DISCRETE-TIME PHASE LOCKED LOOP (PLL)

L. Brecher, N. Sommer, E. Weinstein, Texas Instruments, Herzlia, Israel.

Lock-loss phenomena were studied extensively for continuous-time phase locked loop (PLL), and closed form analytical expressions for the mean time to lose lock (MTLL) has been derived under the assumptions that the input is a phase modulated sine wave, and that the additive noise associated with the input can be added to the detector output. The analysis of the discrete-time phase detector is more complicated as the associated discrete-time stochastic equation depends on the signal constellation as well as on the detector non-linearity. In this study we present an approach for analyzing lock-loss events and for calculating the MTLL in first-order discrete-time PLL, and prove that the time to lose lock is approximately exponentially distributed.

TB4.5

IMPLEMENTATION OF THE BERLEKAMP-MASSEY ALGORITHM USING

DSP, S. Greenberg, N. Feldblum, G. Melamed, Motorola Semiconductor Israel, Omer, Israel.

Abstract - Reed-Solomon (RS) codes are error-correcting codes used in many of today's communication systems. RS encoding and decoding are typically implemented using dedicated hardware elements. In this paper we propose

using software in lieu of a hardware-based RS de-coder. This is accomplished using the Berlekamp-Massey algorithm, implemented on a programmable DSP. This software-based RS decoder using Berlekamp-Massey is implemented on Motorola's MSC8101 StarCore DSP. In order to evaluate the algorithm's performance we use the following criteria: computation cost, cycle count, critical paths in the decoding scheme, and error location in the codeword. Furthermore, we examine the effect of changing the RS code's k , t parameters and its primitive polynomial in real-time implementation. The Berlekamp-Massey algorithm operates over finite field arithmetic, whose steps, as applied on the StarCore DSP, are discussed in detail and specifically evaluated using the assembly code for the syndrome search. We conclude that the Berlekamp-Massey algorithm, used for RS decoding, should be implemented using long code words.

TC4: INTERCONNECT DESIGN

Tuesday, December 14

Time: 16:00 – 17:40

Hall: Tabor

Chair: **A. Baric**, University of Zagreb, Croatia / **A. Kolodny**, Technion, Haifa, Israel.

TC4.1

DESIGN AND MODELLING OF NETWORK ON CHIP INTERCONNECTS USING TRANSMISSION LINES, *A. Barger, *D. Goren, **A. Kolodny, *IBM,

Haifa, Israel, **Technion, Haifa, Israel.

This paper presents an approach to physical design and modeling of Network-on-Chip Interconnects using on-chip transmission lines. Design guidelines are presented allowing the use of simple models with frequency-independent RLCG parameters. Circuit simulation results demonstrate the validity of this approach in a real design environment.

TC4.2

SIGNAL PROPAGATION WITHOUT DISTORTION IN DISPERSIVE LOSSY MEDIA, R. H. Flake, J. Biskup, The University of Texas at Austin, Austin, TX,

USA.

A non-sinusoidal waveform called Speedy Delivery that does not undergo shape distortion during propagation in dispersive lossy media is the subject of this paper. The propagation properties of the waveform and applications of the signal in computer circuits are discussed.

TC4.3

OPTIMAL RESIZING OF BUS WIRES IN LAYOUT MIGRATION, *S. Wimer,

**A. Kolodny, **S. Michaely, *Intel, Haifa, Israel, **Technion, Haifa, Israel.

The effect of wire delay on circuit timing typically increases when an existing layout is migrated to a new generation of process technology, because wire resistance and cross capacitance become more important with scaling. In this paper timing optimization of signal busses is performed by resizing and spacing individual bus wires, while the total area of the whole bus structure is regarded as a fixed constraint. Properties of optimal bus layout are proven, and an iterative algorithm to find the optimal wire widths and spaces is presented. Examples of solutions are shown. Guidelines for design are derived from these results.

TC4.4

BUFFER SIZING FOR DELAY UNCERTAINTY INDUCED BY PROCESS VARIATIONS, *D. Velenis, *R. Sundaresha, **E. G. Friedman, *Illinois Institute of Technology, Chicago, IL, USA, **University of Rochester, Rochester, NY, USA.

Controlling the delay of a signal in the presence of various noise sources, process parameter variations, and environmental effects represents a fundamental problem in the design of high performance synchronous circuits. The effects of device parameter variations on the signal propagation delay of a CMOS buffer are described in this paper. It is shown that delay uncertainty is introduced due to variations in the current flow through a buffer. In addition, the variations in the parasitic resistance and capacitance of an interconnect line also affect the buffer delay. A design methodology that reduces the delay uncertainty of signals propagating along buffer-driven interconnect lines is presented. The proposed methodology increases the current flow sourced by a buffer to reduce the sensitivity of the delay on device and interconnect parameter variations.

TC4.5

OPTIMIZATION OF CHIP LEVEL CLOCK TREE PERFORMANCE BY USING

SIMULTANEOUS DRIVERS AND WIRE SIZING, S. Greenberg, I. Bloch, A. Maman, M. Horowitz, Motorola Semiconductor Israel, Omer, Israel, Ben-Gurion University, Beer-Sheva, Israel.

Abstract - Defining the optimal clock-distribution network in VLSI is one of the most important aspects of high-speed SoC design. The existing flows of a clock tree network implementation are manual based and require long development time. This long and iterative flow is not optimized in terms of: Clock-skew, insertion delay, clock signal degradation, power dissipation, route area, sensitivity to process/design variations and time to market. This paper demonstrates that using preliminary HSPICE simulations we can dramatically improve the clock tree performance by smartly choosing the following parameters: number of driver's levels, driver's size, wire width/space and wire length between levels. We applied this approach to the chip level clock tree network of the new Motorola Semiconductor MSC8122 Quad Core DSP (500Mhz, 90nm CMOS technology, 0.9686cm X 1.1792cm die size). This results in saving 12% power dissipation and 15% route area by route changing, without any decrease in performance.

TD4: MICRO-OPTO-ELECTRO-MECHANICAL SYSTEMS

Tuesday, December 14

Time: 16:00 – 17:40

Hall: Arbel

Chair: **J. G. Harris**, University of Florida, Gainesville, FL, U.S.A / **R.**

Shavit, Ben-Gurion University, Beer-Sheva, Israel

TD4.1

2D PHOTONIC CRYSTALS DEPOSITED ON POLYMER PIEZOELECTRIC SUBSTRATES - NEW KIND OF MOEMS, E. Bormashenko, R. Pogreb, O.

Stanevsky, Y. Biton, Y. Bormashenko, V. Streltsov, Y. Socol, The College of Judea and Samaria, Ariel, Israel.

Self-assembled polycarbonate films were deposited on polymer piezoelectric substrates under a fast dip-coating process. Ordered structures with micro- and nano-scaled holes dispersed in the polycarbonate matrix were obtained, demonstrating 2D hexagonal packaging. Fabricated structures have a potential as 2D tunable photonic crystals. A distinct bandgap in the near IR was revealed. Integration of photonic bandgap structure with MOEMS was achieved.

TD4.2

A METHOD TO DESIGN DWDM FILTERS ON PHOTONIC CRYSTALS, A.

Perri, A. Giorgio, R. Diana, Polytechnic of Bari, Bari, Italy.

A new very promising technology for Dense Wavelength Division Multiplexing (DWDM) systems seems to be the Photonic Crystals with forbidden bandgap (Photonic Band-Gap, PBG). In this paper we propose a method for the design of DWDM filters on PBG based on a new model developed by the authors and already described.

TD4.3

A NOVEL DESIGN AND FABRICATION METHOD OF SCANNING MICRO-MIRROR FOR RETINAL SCAN DISPLAYS, O. Cohen, Y. Nemirovsky,

Technion, Haifa, Israel.

In this paper we present a novel scheme for designing and fabricating a single axis scanning micro mirror. The device is a match of two chips with a flip chip bonder. In this paper we describe mostly the top chip that include the reflecting surface. The device is very low cost and electrostatic actuated in relatively low voltage. We present in this paper the fabrication process scheme based on wet etching of silicon wafers. We also present in this paper the motivation to

use thin wafers as much as 50 μ m thick to reach resonant frequency of 15-30KHz suitable for raster scanners such as retinal scan displays. At last we present a preliminary outcomes of such a process.

TD4.4

A NOVEL DESIGN AND FABRICATION METHOD OF A PYRAMIDAL SHAPE CHIP FOR SCANNING MICRO MIRROR, O. Cohen, A. Shai, Y. Nemirovsky, Technion, Haifa, Israel.

In this paper we present a novel scheme for designing and fabricating a base chip, which is an approximation of pyramid shape, and is not limited by the natural slope of 54.7 degrees obtained with wet anisotropic etching of silicon. The application for such a pyramid shape in our case is for single axis scanning micro mirror. The paper presents the methodology for designing and fabricating a surface with an arbitrary slope, as required by the application. In our case, it is an approximation of a desired very moderate slope. The moderate slope is serving as electrostatic actuator with relatively low operating voltage. On top of the base we bond a mirror chip that includes the opposite side of the actuator, the reflector of the mirror, the mechanical structure of the mirror and the hinges. We present in this paper the motivation to use a pyramidal shaped base. The design is simple and requires knowledge of etch rates in several crystal planes, which can be easily measured. The fabrication tools and methods used herein are based on wet etching of silicon wafers. There is no need for DRIE processes or SOI wafers.

TD4.5

COMPACT RF-PHOTONIC CONFIGURATION FOR HIGHLY RESOLVED AND ULTRAFAST EXTRACTION OF CARRIER AND INFORMATION OF RADAR SIGNAL, *Z. Zalevsky, **A. Shemer, ***V. Eckhouse, ***D. Mendlovic, **** S. Zach *Bar-Ilan University, Ramat-Gan, Israel, **Tel-Aviv University, Tel-Aviv, Israel, ***Civcom Devices and Systems Inc., Petah-Tikva, Israel, **** Walles.

In this paper we present a highly resolved carrier and information extraction of optically modulated RADAR signal. The extraction is done by passing the optical beam through a monitoring path that realizes finite impulse response filter. Replications of the monitoring signal realize the required spectral scan of the filter. Despite the fact that the filter configuration is fixed, each replication experiences different spectral filtering. The RADAR carrier is detected by observing the energetic fluctuations in low rate output detector. The RF information is extracted by positioning low rate tunable filter at the detected carrier frequency.

WA1: SOC DESIGN AND INTEGRATION

Wednesday, December 15

Time: 9:00 – 10:40

Hall: Galil

Chair **Y. Betser**, Saifun, Netanya, Israel.

WA1.1

AUTOMATIC HARDWARE-EFFICIENT SOC INTEGRATION BY QOS

NETWORK ON CHIP, E. Bolotin, A. Morgenshtein, I. Cidon, R. Ginosar, A. Kolodny, Technion, Haifa, Israel.

Efficient module integration in Systems on Chip (SoC) is a great challenge. We present a novel automated Network on Chip (NoC) centric integration method for large and complex SoCs. A Quality of Service NoC (QNoC) architecture and its design considerations are presented. Then we describe a chain of design automation tools that allows fast and hardware-efficient SoC integration using the QNoC paradigm. The tool-chain receives a list of system modules and their inter-module communication requirements and results in a complete system hardware and verification models for faster SoC fabrication and easier verification.

WA1.2

MICRO-MODEM RELIABILITY SOLUTION FOR NOC COMMUNICATIONS,

A. Morgenshtein, E. Bolotin, I. Cidon, A. Kolodny, R. Ginosar, Technion, Haifa, Israel.

A new concept of Micro-Modem interface for reliable communications in Networks on Chip (NoC) is presented. The Micro-Modem addresses the major problems of sub-micron interconnect and contains techniques for reliability improvement. The architecture, data flow and components of the Micro-Modem are presented. Various techniques and processes are analyzed for compact on-chip implementation. Design and application considerations are discussed.

WA1.3

PRACTICAL PERFORMANCE OF PLANAR SPIRAL INDUCTORS,

A. Telli, METU, Ankara, Turkey.

The inductors are essential elements for RF design. For RFIC design, bondwires, planar solenoidal and planar spiral inductors are available. Due to some limitations of bondwires and planar solenoidal inductors, planar spiral inductors are the most popular ones. The designers try to get accurate lumped

element models for modeling planar spiral inductors to be able to simulate the circuit performance correctly before getting the integrated circuit manufactured. In this study, planar spiral inductors measurement methods have been discussed, and the comparison between lumped element model simulation results and experimental measurement results have been given. The results of this study show that it is possible to model planar spiral inductors with lumped element circuit models parameters of which can be calculated by basic but accurate expressions.

WA1.4

CRITERION OF DESIGN FOR SMALL VALUE INTEGRATED SELF-INDUCTORS, * '***G. Petit, *R. Kielbasa, **V. Petit, *Supelec, Gif sur Yvette, France, **Thales Airborne Systems, Elancourt, France.

Facing the increase in frequency of use of analog products, integrated-circuits designers reach X or upper band and their own problems, especially in the case of passive components. This paper focus on inductor design and layout, opposing classical analog integrated inductors and hyper frequency lines. After studying separately each solution and pointing out their limits on an actual SOS 0.5um case, a methodology to solve this issue is exposed and a choice criterion is supplied.

WB1: IMAGE AND VISION SYSTEMS

Wednesday, December 15

Time: 9:00 – 10:40

Hall: Carmel

Chair: **S. Greenberg**, Freescale Semiconductor, Israel / **N. Intrator**, Tel-Aviv university, Tel-Aviv, Israel

WB1.1

IMAGE REGISTRATION AND MOSAICING OF NOISY ACOUSTIC CAMERA IMAGES, K. Kim, N. Intrator, N. Neretti, Brown University, Providence, RI, USA

We introduce an algorithm for image registration and mosaicing on underwater sonar image sequences characterized by a high noise level, inhomogeneous illumination and low frame rate. For a planar surface viewed through a pinhole camera undergoing translational and rotational motion, registration can be obtained via a projective transformation. For an acoustic camera, we show that, under the same conditions, an affine transformation is a good approximation. We propose a novel image fusion, which maximizes the signal-to-noise ratio of the mosaic image. The full procedure includes illumination correction, feature based transformation estimation, and image fusion for mosaicing.

WB1.2

DESIGN OF LOW CROSS-TALK IMAGE TRANSCEIVER DEVICE AND CONTROLLER CIRCUITRY, U. Efron, Y. David, I. Baal-Zedaka, N. Thirer, Ben-Gurion University, Beer-Sheva, Israel, Holon Academic Institute of Technology, Holon, Israel

An Image Transceiver Device (ITD) is under development at the Holon Institute and Ben-Gurion University. The device, capable of performing imaging and display functions in a single chip, is based on a combination of CMOS and LCOS technologies. Its main applications include Smart Goggle and Vision enhancement. In this paper we report on studies to reduce the cross talk in the ITD chip. These studies which cover an n-well, a twin-well and a deep p-well structure, indicate that the deep p-well structure is the preferred approach resulting in the lowest cross-talk level of all 3 candidates. The second area studied was a novel design of an FPGA chip required in order to control the unique Imager-Display circuitry of the ITD. Details of the controller circuitry and its functions are presented.

WB1.3

ISFET CMOS COMPATIBLE DESIGN AND ENCAPSULATION

CHALLENGES, L. Sudakov-Boreysha, A. Morgenshtein, U. Dinnar, Y. Nemirovsky, Technion, Haifa, Israel

This work shows main challenges in ISFET encapsulation. It analyzes SU8 drawbacks as an encapsulant and presents a novel flip-chip bonding packaging concept.

WB1.4

COMPUTER AIDED DESIGN USING CGH OF A THREE-DIMENSIONAL OBJECTS

D. Abookasis, J. Rosen, Ben-Gurion University, Beer-Sheva, Israel

A new method of synthesizing computer-generated holograms of three-dimensional (3-D) objects is proposed. Several projections of the 3-D object are numerically processed to yield a two dimensional complex function, which is then encoded as a computer-generated hologram. When this hologram is illuminated by a plane wave, a 3-D real image of the object is reconstructed. Although the hologram initially belongs to the type of Fourier holograms, Fresnel and image holograms are also generated by computing the propagation of the wave front from the Fourier plane to any other desired plane. Computer and optical constructions of 3-D objects, both of which show the feasibility of the proposed approach, are presented herein.

WB1.5

VLSI SENSOR FOR MULTIPLE TARGETS DETECTION AND TRACKING

*A. Fish, *A. Spivakovsky, *A. Goldberg, *, **O. Yadid-Pecht, Ben-Gurion University, Beer-Sheva, Israel, University of Calgary, Alberta, Canada.

An architecture for implementation of a novel tracking VLSI sensor for multiple targets detection and tracking is presented. The sensor, based on the proposed implementation concept allows acquisition and real time tracking of up to three bright targets in the field of view. While based on the spotlight model of visual attention in biological systems, the proposed sensor features several advantages. This includes distractors elimination, attentional shifts possibility with no dependence on the distance between the targets of interest, high quality image in the snapshot mode of operation simultaneously with tracking and low-power dissipation. A comparison of the proposed concept to the existing spotlight and object-based visual attention models is discussed and a brief description of the proposed sensor is given.

WC1: DESIGN FOR TESTABILITY AND RELIABILITY

Wednesday, December 15

Time: 9:00 – 10:40

Hall: Tabor

Chair: **Y. Rosenwaks**, , Tel-Aviv University, Tel-Aviv, Israel

WC1.1

FAST HIGH-LEVEL FAULT SIMULATOR, K. Sapiecha, S. Deniziak, Cracow University of Technology, Cracow, Poland.

In this paper a new fast fault simulation technique is presented for calculation fault propagation through High Level Primitives (HLPs). Reduced Ordered Ternary Decision Diagrams are used to describe HLPs. The technique is implemented in HTDD fault simulator. The simulator is evaluated with some ITC99 benchmarks. Besides high efficiency (in comparison with existing fault simulators) it shows flexibility for adoption of wide range of fault models.

WC1.2

AUTOMATIC SYSTEM FOR VLSI ON-CHIP CLOCK SYNTHESIZERS CHARACTERIZATION, Y. Fefer, S. Sofer, Motorola Semiconductor Israel Ltd., Herzeliya, Israel.

Analyzing the ability of clock generation circuits to provide high quality chip clock for synchronous systems is very critical. This is important in order to ensure stable functioning of such systems at highest frequencies and reliable communication between core and on-chip peripherals to external peripherals and memory. We propose clock synthesizer characterization system, which performs automatic measurements of the clock synthesizer's parameters at various modes, frequencies, power supply voltages, ambient temperatures, and also in quiet and in noisy environments. Accuracy of the measurements together with high flexibility and speed of the system, allow performing on the spot characterization, resulting in a detailed and statistically reliable picture of clock signal's quality. Practical experience shows efficiency and importance of the system for clock synthesizer characterization as well as for failure analysis.

WC1.3

INVESTIGATION OF ON-CHIP PLL IRREGULARITIES UNDER STRESS CONDITIONS CASE STUDY, Y. Fefer, Y. Weizman, S. Sofer, E. Baruch, Motorola Semiconductor Israel Ltd., Hertzliya, Israel.

In modern high performance VLSI design, On-chip Phase Locked Loop (PLL) performance degradation due to intensive core switching activities is becoming an influential factor. Under certain borderline conditions, the PLL may become unstable. The analysis herein describes PLL irregularities under marginal mode, frequency and voltage conditions combined with intensive core operations. After lengthy analysis that included step-by-step elimination of all noise sources, a cause of PLL instability was attributed to coupling between a voltage spike on core power supply line and the internal control signal of the voltage controlled oscillator of the PLL through the chip substrate. Solution to the problem was suggested by changing the PLL dynamic characteristics. Through this investigation we studied the noise cross-talk issue in mixed mode (analog and digital) systems and also the PLL dynamics under stress conditions, which demonstrates the complexity of PLL analysis in a System on Chip environment.

WC1.4

ON-CHIP AREA-EFFICIENT SPECTRUM ANALYZER FOR TESTING

ANALOG IC, *M. A. *Dominguez, *J. L. Ausin, **G. Torelli, *J. F. Duque-Carrillo, *University of Extremadura, Badajoz, Spain, ** University of Pavia, Pavia, Italy.

This paper presents an effective approach to the design of on-chip spectrum analyzers based on switched-capacitor (SC) techniques. High programmability resolution is obtained by using a non-uniform sampling scheme without modifying any capacitor value. As a result, capacitor spread and total capacitor area are reduced as compared to traditional solutions and, hence, test area overhead can be minimized. To prove the feasibility of the proposed approach, the design and the implementation of a 0.35- μm CMOS SC spectrum analyzer are discussed. Simulation results confirm that high measurement accuracy can be achieved.

WD1: SPECIAL SESSION - RE-INVENTING METHODS AND TOOLS FOR NEXT-GENERATION CMOS DESIGN

Wednesday, December 15

Time: 9:00 – 10:40

Hall: Arbel

Chair: **H. Yeshurun**, TAU, Tel Aviv, Israel.

WD1.1

PERSPECTIVES ON SCALING THEORY AND CMOS TECHNOLOGY: UNDERSTANDING THE PAST, PRESENT, AND FUTURE, PART I, D. Foty, Gilgamesh Associates, Fletcher, VT, USA.

In this paper, the critical importance of scaling theory to the success of CMOS technology will be reviewed and evaluated. The history of CMOS shows that scaling theory has been the dominant theme, but that the evolution of the technology has followed different directions at different times due to constraints imposed by scaling theory. The state of present-day constraints will be considered, followed by discussion of some possible options for continuing the progress of CMOS into the future.

WD1.2

PERSPECTIVES ON SCALING THEORY AND CMOS TECHNOLOGY: UNDERSTANDING THE PAST, PRESENT, AND FUTURE, PART II, D. Foty, Gilgamesh Associates, Fletcher, VT, USA.

WD1.3

ADVANCED COMPACT MODELS: GATEWAY TO MODERN CMOS DESIGN, PART I, *G. Gildenblat, **C. McAndrew, *H. Wang, *W. Wu, ***D. Foty, ****L. Lemaitre, *****P. Bendix, *The Pennsylvania State University, University Park, PA, USA, **Motorola Inc., Tempe, AZ, USA, ***Gilgamesh Associates, Fletcher, VT, USA, ****Motorola Inc., Geneva, Switzerland, *****LSI Logic Corporation, Milpitas, CA, USA.

Recent progress in MOS device physics, model development, and model implementation process has qualitatively changed the capabilities of compact models precisely at a time when the rapid expansion of RF MOSFET applications is imposing the most stringent demands on the new generation of MOSFET models. This work reviews the impact of the new modeling paradigm on MOSFET circuit simulation with particular attention to RF issues, non-quasi-static effects, and symmetric surface-potential-based models. General

principles are illustrated with the simulation results using the latest generation compact MOSFET model (SP).

WD1.4

ADVANCED COMPACT MODELS: GATEWAY TO MODERN CMOS DESIGN, PART II

*G. Goldenblat, **C. McAndrew, *H. Wang, *W. Wu, ***D. Foty, ****L. Lemaitre, *****P. Bendix, *The Pennsylvania State University, University Park, PA, USA, **Motorola Inc., Tempe, AZ, USA, ***Gilgamesh Associates, Fletcher, VT, USA, ****Motorola Inc., Geneva, Switzerland, *****LSI Logic Corporation, Milpitas, CA, USA.

WD1.5

PRACTICAL ASPECTS OF MOS TRANSISTOR MODEL “ACCURACY” IN MODERN CMOS TECHNOLOGY

*P. Bendix, **D. Foty, *D. Pachura, *LSI Logic Corporation, Milpitas, CA, USA, ** Gilgamesh Associates, Fletcher, VT, USA.

In this paper, model “accuracy” is considered from a more practical and wide-ranging viewpoint. First, binned and unbinned models are compared – with particular emphasis on “accuracy” as it relates to the process center, rather than fitting results for one specific set of measured data. Next, that discussion is extended to the generation of digital timing libraries. The frightening increase in model complexity is usually justified as being necessary to provide “sufficient accuracy” for modern digital design; however, we find that much simpler model forms provide very suitable results, without the costs and baggage associated with very complex models. This leads to some surprising conclusions regarding the true costs and benefits of model “accuracy,” and also to the identification of a sharp divergence between the MOS modeling needs of analog design and digital design.

WA2: HIGH PERFORMANCE ARCHITECTURES

Wednesday, December 15

Time: 11:00 – 12:40

Hall: Galil

Chair: **M. Werner**, Technion, Haifa, Israel

WA2.1

A HIGH PERFORMANCE DATA-PATH TO ACCELERATE DSP KERNELS,

M. Galanis, C. Goutis, University of Patras , Patras, Greece.

In this paper, a high-performance data-path for accelerating DSP kernels is proposed. The data-path is based on a flexible, universal, and regular component that allows to optimally exploiting both inter- and intra-component chaining of operations. The component is implemented as combinational circuit and the steering logic existing inside the component allows to easily realizing any desirable complex hardware unit - called template - so that the data-path's performance benefits from the chaining of operations. Due to universal structure of the component, the synthesis of an application is accomplished by efficient algorithms. An average reduction of 20% in latency cycles is achieved when a comparison with a template-based data-path is performed.

WA2.2

A 64-WAY VLIW/SIMD FPGA PROCESSING ARCHITECTURE AND

DESIGN FLOW, A. K. Jones, R. Hoare, I. Kourtev, J. Fazekas, D. Kusic, J. Foster, S. Boddie, A. Muaydh, University of Pittsburgh, Pittsburgh, PA, USA.

Current FPGA architectures are heterogeneous, containing tens of thousands of logic elements and hundreds of embedded multipliers and memory units. However, efficiently utilizing these resources requires hardware designers and complex computer aided design tools. This paper describes several multi-processor architectures implemented on a FPGA including a 64-way single interface multiple data (SIMD) and variable size very long instruction word (VLIW) architecture. The design and synthesis of the target architectures are presented and compared for scalability and achieving parallelism. The performance and chip utilization of a shared register file is examined different numbers of VLIW processing elements. The associated compilation flow is described based on the Trimaran VLIW compiler which achieves explicitly parallel instructions from C code. Benchmarks from the Media-Bench suite are being used to test the performance of the parallelism of both the software and hardware components.

WA2.3

THE 1:10 PHASED DEMULTIPLEXER CIRCUIT, S. Poriazis, Phasetronic Laboratories, Athens, Greece.

The behavior of the 1:10 Phased Demultiplexer (PDMUX10) circuit is analyzed. The circuit demultiplexes the input clock signal into ten phased output signals by streaming sets of twenty clock phases. A phase difference equal to the half period of the clock is maintained between consecutive output transitions. The VHDL description of the PDMUX10 cell is given and the simulation and synthesis results are generated. A 2-level tree-like structure is built by applying the phased outputs of the PDMUX10 cell into the corresponding clock inputs of ten cell replicas that extend the circuit behavior. The EXOR10 gate is attached to the PDMUX10 cell output ports and is aggregating all the phases that the phased clock signals are carrying while preserving their phase associations.

WA2.4

SYSTEMC OPPORTUNITIES IN CHIP DESIGN FLOW, I. Yarom, G. Glasser, Intel, Jerusalem, Israel.

Moore law predicts that the numbers of transistor will double every 18 months. However, in order to take advantage of the chip technology progress, the same progress needs to be done in the chip design process. In this paper we will focus on the benefit of the SystemC technology in order to close this gap. We will present research done in Intel Development Center (IDC) with Tel-Aviv University (TAU) and Jerusalem College of Technology (JCT). The research explores different usages of SystemC in design and verifications flow, which includes: soft system verification (early in the design flows), architecture tradeoffs and a flow of SystemC to gate-level flow.

WB2: DIGITAL SIGNAL PROCESSING

Wednesday, December 15

Time: 11:00 – 12:40

Hall: Carmel

Chair: **R. J. Chen**, National United University, Miao City, Taiwan / **H. Aharoni**, Ben-Gurion University of the Negev, Israel.

WB2.1

HIGH SPEED ASSEMBLY FFT IMPLEMENTATION FOR MEMORY ACCSS REDUCTION ON DSP PROCESSORS, ^{*}Y. Tang, ^{*}Y. Wang, ^{**}J. G. Chung, ^{**}S. Song, ^{**}M. Lim, ^{*}University of Texas at Dallas, Richardson, TX, USA, ^{**}Chonbuk National University, Chonju, South Korea

Memory reference in digital signal processors (DSP) is among the most costly operations due to its long latency and substantial power consumption. Previously proposed twiddle-factor-based butterfly grouping method can effectively minimize memory references due to twiddle factors for implementing any fast Fourier transform (FFT) algorithms on DSP. However, the performance of its C implementation on DSP is far behind the performance of TI assembly benchmark for FFT due to the inefficiency of the compiler. In this paper, we further propose a hand-coded assembly implementation for radix-2 DIF FFT with twiddle-factor-based butterfly grouping method on TI TMS320C64x DSP. Experimental results show that for 1024-pt radix-2 DIF FFT, our hand-coded assembly is 8 times faster than the C implementation and a little bit faster than the TI assembly benchmark while requiring only 1/10 memory references compare to the TI assembly benchmark.

WB2.2

VITERBI DETECTION ANALYSIS ON RLL SEQUENCES, P. M. Putinica, S. Stancescu, University Politehnica Bucharest, Bucharest, Romania

This paper presents partial response equalization and detection methods based on maximum likelihood (PRML) with the purpose of analyzing detection process in function of the sequence coding in a recording magnetic channel. A channel simulator tests equalization, detection and decoding alternatives, under channel and noise characteristic variations. The paper presents a Viterbi detector and compares its Bit Error Rate-BER performances using random or Run Length Limited RLL encoded data sequences, with the already existing solutions.

WB2.3

RECONSTRUCTION OF NONUNIFORMLY SAMPLED PERIODIC

SIGNALS: ALGORITHMS AND STABILITY ANALYSES, E. Margolis, Y. C. Eldar, Technion, Haifa, Israel

This paper introduces two new algorithms for perfect reconstruction of a periodic bandlimited signal from its nonuniform samples. We analyze the advantages and disadvantages of each method and discuss their properties. Based on the theory of frames, we also analyze the stability of the algorithms. Some special structures of the sampling points are investigated and we show that uniform sampling results in the most stable and simple reconstruction algorithm. We also provide experimental evidence to support our theoretical results.

WB2.4

MINIMAX SAMPLING WITH ARBITRARY SPACES, T. Dvorkind, Y. C. Eldar, Technion, Haifa, Israel

We consider non-ideal sampling and reconstruction schemes in which the sampling and reconstruction spaces as well as the input signal can be arbitrary. To obtain a good reconstruction of the signal in the reconstruction space from arbitrary samples, we suggest processing the samples prior to reconstruction with a linear transformation that is designed to minimize the worst-case squared-norm error between the reconstructed signal, and the best possible (but usually unattainable) approximation of the signal in the reconstruction space. We show both theoretically and through a simulation that if the input signal does not lie in the reconstruction space, then this method can outperform the consistent reconstruction method previously proposed for this problem.

WB2.5

A STATISTICAL TECHNIQUE FOR THE DETERMINATION OF THE NOISE POWER GAIN IN HIGHER-ORDER SIGMA-DELTA A/D CONVERTERS

EXCITED BY DC INPUT SIGNALS, B. Nowrouzian, N. A. Fraser, University of Alberta, Edmonton, Alberta, Canada.

The existing techniques available for the statistical determination of the noise power gain (NPG) in general-order sigma-delta (SD) A/D converters are based on the assumption that the quantizer input signal has a Gaussian distribution. However, empirical investigations reveal that this assumption holds true for the special cases of the conventional first and second-order SD A/D converters only. This paper presents an alternative technique for a more accurate determination of NPG for higher-order SD A/D converters excited by DC input signals. This is achieved by employing the Gram-Charlier series for a (quasi-

linear) modeling of the quantizer input signal. The proposed technique is based on the practical assumption that the constituent quantizer operates in its overload-free region. A typical practical application example is given to illustrate the main results.

WC2: SEQUENTIAL SYNTHESIS METHODOLOGIES

Wednesday, December 15

Time: 11:00 – 12:40

Hall: Tabor

Chair: **D. Lubzens**, Technion, Haifa, Israel.

WC2.1

LURU: TIME-OPTIMIZED FPGA TECHNOLOGY MAPPING WITH CONTENT ADDRESSABLE MEMORIES, A. K. Jones, J. Lucas, R. Hoare, I. Kourtev, University of Pittsburgh, Pittsburgh, PA, USA.

This paper proposes a technique for area-optimized FPGA technology mapping. The LURU algorithm maps a combinational circuit to a network of K-input lookup tables (LUTs). The LURU algorithm uses content addressable memory (CAM) to enable parallel pattern matching in a Boolean network. As a result, it is possible to quickly perform global searches within an entire Boolean network, thus increasing the quality of results compared to algorithms of local scope. To utilize CAM for the LURU algorithm, a circuit is described as a set of one dimensional text strings, each of which independently represents the topology of a portion of the circuit. The LURU algorithm was tested with specially partitioned circuits from the ISCAS '85 set of combinational benchmarks. These results are compared with results obtained from the mapping algorithms FlowMap and CutMap. It is demonstrated that using LURU leads to an average of 25% area improvement over both FlowMap and CutMap.

WC2.2

ADVANCED TIMING OF LEVEL-SENSITIVE SEQUENTIAL CIRCUITS, B. Taskin, I. Kourtev, University of Pittsburgh, Pittsburgh, PA, USA.

This paper addresses the advanced timing analysis of multi-phase level-sensitive synchronous circuits under clock skew scheduling. The timing analysis framework previously offered for a single-phase clocking scheme is enhanced to accommodate a multi-phase clocking scheme. In particular, the timing analysis framework is used to formulate the clock period minimization problem of multi-phase level-sensitive circuits. The modified big M method is used to linearize the formulation of the clock period minimization problem and experiments are performed on the ISCAS'89 benchmark circuits. In single-phase level-sensitive circuits, up to 63% improvements over conventional zero clock skew, edge-triggered circuits are achieved through the simultaneous application of non-zero clock skew scheduling and time borrowing.

Comparable improvements up to 62% are achieved for the same circuit topologies under a multi-phase clocking scheme.

WC2.3

PERFORMANCE IMPROVEMENT OF EDGE-TRIGGERED SEQUENTIAL CIRCUITS, B. Taskin, I. Kourtev, University of Pittsburgh, Pittsburgh, PA, USA.

This paper presents a novel delay insertion method to prove the performance of edge-triggered sequential circuits through clock skew scheduling. Clock skew scheduling (CSS) is performed on synchronous circuits in order to increase the maximum operating frequency. With CSS, the original circuit topology is preserved while the clock distribution network is modified to satisfy an optimal clock skew schedule. The work presented here proposes a circuit modification technique consisting of delay insertion into logic paths in order to improve the minimum possible clock period. In experiments, improvements of up to 90% are observed over the zero clock skew, flip-flop based circuits for the selected ISCAS'89 suite of benchmark circuits.

WC2.4

DESIGN OF DOUBLY COMPLEMENTARY FILTER PAIRS WITH CANONICAL SIGNED-DIGIT COEFFICIENTS USING GENETIC ALGORITHM, L. Liang, M. Sid-Ahmadi, University of Windsor, Windsor, Canada.

In this paper, a genetic algorithm (GA) is used to design doubly complementary filter pairs, which are realized as a parallel connection of two all-pass filters. The designed filters have Canonical Signed-Digit (CSD) coefficients. A new CSD number restoration technique is proposed to ensure that the algorithm generates CSD coefficients with the pre-specified wordlength and maximum number of non-zero digits.

WD2: IMAGE PROCESSING

Wednesday, December 15

Time: 11:00 – 12:40

Hall: Arbel

Chair **A. Morgenshtein**, Technion, Haifa, Israel

WD2.1

A ROBUST AND FAST MODEL-BASED ATHLETE CONTOUR TRACKING IN DIVING VIDEOS, Y. Xiong, Y. Zhang, D. Yao, Tsinghua University, Beijing, China.

This paper presents a novel tracking scheme to detect the athlete contour in diving videos, which is an important step in on-line motion analysis of diving training. This scheme is mainly based on the active contour model in linear shape space. First, an initial template is built on the first frame of the diving video and is updated by a curve-fitting algorithm. Then in each following frame, the template transforms and adjusts itself to track the athlete contour, according to the information from both prior model knowledge and current frame analysis. Meanwhile, the changes of template between frames are detected and recorded to improve the efficiency of process in the following frames. Finally, the athlete contour is tracked out frame by frame and experiments demonstrate that the proposed scheme is both efficient and robust for the athlete contour tracking in diving videos.

WD2.2

EFFICIENT GABOR EXPANSION USING NON MINIMAL DUAL GABOR WINDOWS, Nagesh K. Subbanna, Yonina Eldar, Technion, Haifa, Israel.

In this paper, we illustrate the computational advantages of a class of non minimal dual Gabor frames over the minimal dual Gabor frame. Specifically we demonstrate that using the non minimal frames can lead to Gabor expansions that can be computed far more easily than the traditional expansions. Several properties of these non minimal Gabor frames are mentioned and some necessary and sufficient conditions are derived for the existence of this class of non-minimal duals.

WD2.3

EFFICIENT LDPC CODES FOR JOINT SOURCE-CHANNEL CODING, H. Kfir, I. Kanter, Bar-Ilan University, Ramat-Gan, Israel.

Belief Propagation (BP) decoding of LDPC codes is extended to the case of Joint Source-Channel coding. The uncompressed source is treated a Markov process, characterized by a transition matrix, T , which is utilized as side

information for the Joint scheme. The method is based on the ability to calculate a prior for each decoded symbol separately, and re-estimate this prior dynamically after every iteration of the BP decoder. We demonstrate the implementation of this method using MacKay and Neel's LDPC algorithm over GF(q), and present simulation results indicating that the proposed scheme is competitive with separate coding, even when advanced compression algorithms (such as AC, PPM) are used. The extension to 2D (and higher) arrays of symbols is straight-forward. Finally, the ability of using the proposed scheme with the lack of side information is briefly sketched.

WD2.4

ULTRA LOW-POWER DFF BASED SHIFT REGISTERS DESIGN FOR CMOS IMAGE SENSORS APPLICATIONS, *A. Fish, *V. Mosheyev, *V.

Linkovsky, *, **Orly Yadid-Pecht, *Ben-Gurion University, Beer-Sheva, Israel, **University of Calgary, Alberta, Canada.

Various implementations of D-Flip-Flops (DFF) for shift register designs in CMOS image sensors are proposed. Driven by requirements of low-area and low-power dissipation, the presented FFs allow implementation of power-efficient shift registers, used for signal readout control and windows of interest definition in CMOS image sensors and are optimized for operation at low frequencies. Power dissipation of the presented DFFs is significantly reduced by leakage control using the stack effect. A variety of DFFs and a shift-register, using the stacking effect approach, have been implemented in 0.18 μ m standard CMOS technology to compare the proposed DFFs and shift-register structures with existing alternatives, showing an up-to 63% reduction in power dissipation of a shift-register at 30Hz frequency. Operation of the proposed circuits is discussed and simulation results are reported.

WA3: ADVANCED SYNTHESIS AND VERIFICATION METHODOLOGIES

Wednesday, December 15

Time: 14:00 – 15:40

Hall: Galil

Chair: **I. Yarom**, Intel Corporation, Israel

WA3.1

TECHNIQUES FOR FORMAL TRANSFORMATIONS OF BINARY DECISION DIAGRAMs, *G. Kolotov, **I. Levin, **V. Ostrovsky, *Tel-Aviv University, Tel-Aviv, Israel, **Bar-Ilan University, Ramat-Gan, Israel

Binary Decision Diagrams (BDDs), when used for representation of discrete functions, permit the direct technology mapping into multi-level logic networks. Complexity of a network derived from a BDD is expressed by its number of non-terminal nodes. This paper discusses the problem of reducing the BDDs. The paper has two main contributions: a) bounds of potential complexity of the BDD have been determined and proven; b) a formal technique is presented for simplification of Boolean operations on a set of BDDs.

WA3.2

EVALUATING AND COMPARING SIMULATION VERIFICATION VS. FORMAL VERIFICATION APPROACH ON BLOCK LEVEL DESIGN, *E. Segev, *S. Goldshlager, *H. Miller, *O. Shua, *O. Sher, **S. Greenberg, *Motorola Semiconductor Israel, Omer, Israel, **Ben-Gurion University, Beer-Sheva, Israel

In the last few years the logic design has become very complex in term of logic functionality. System On a Chip (SOC) designs are an integration of multiple modules and cores. In many cases SoC integration is a result of integrating few chips together. Each piece (module or core) must be verified separately (stand alone) prior to chip level verification. Standalone logic verification of the design is one of the most important steps in the overall design effort. Following the increase of the amount of functionality at each module, the logic verification effort has become one of the most resources consuming tasks. Two logic verification methods are commonly used when verifying a SOC: simulation based verification and formal based verification. In this paper the two methods are explored and compared with respect to the time required for setup and running the environment, ease of debugging the reported failures, power, coverage and confidence level. Our main goal is to establish criteria for optimal use of simulation based verification and formal based verification in the verification process and implement both methods on the PCMCIA_IF block. PCMCIA (Personal Computer Memory Card International Association) is a

standard for using memory and I/O devices as insertable, exchangeable peripherals for personal computers. In the current research we derived some important conclusions concerning the matching of these methods for the verification of blocks of a similar type.

WA3.3

PATTERN SEARCH IN HIERARCHICAL HIGH LEVEL DESIGNS, ^{*}Z. Terem, ^{*}G. Kamhi, ^{**}M. Y. Vardi, A. Iרון, ^{*}Intel, Haifa, Israel, ^{**}Rice University, Houston, TX, USA

The main focus of this paper is on using algorithms for design pattern matching to address the challenges of designs at RT and higher abstraction levels. The crux of our approach is modeling designs and patterns as graphs, which lets us express design pattern matching as subgraph isomorphism. We apply a constraint-satisfaction approach and address the problem of both exact and generalized matching. Our experimental results confirm the applicability of our approach on industrial test cases.

WA3.4

META-HEURISTICS HYBRIDIZING INDEPENDENT COMPONENT ANALYSIS WITH GENETIC ALGORITHMS, J. Gorritz, C. G. Puntonet, E. Lang, M. Salmeron, University of Cadiz, Algeciras, Spain.

In this work we present a novel method for blindly separating unobservable independent component signals from their linear mixtures, using meta-heuristics such as genetic algorithms (GA) to minimize the nonconvex and nonlinear cost functions. This approach is very useful in many fields such as forecasting indexes in financial stock markets where the search for independent components is the major task to include exogenous information into the learning machine. The GA presented in this work is able to extract independent components with faster rate than the previous independent component analysis algorithms based on Higher Order Statistics (HOS) as input space dimension increases showing significant accuracy and robustness.

WB3: VLSI CRYPTOLOGY

Wednesday, December 15

Time: 14:00 – 15:40

Hall: Carmel

Chair: **M. Ahmadi**, University of Windsor, Canada.

WB3.1

EFFICIENT IMPLEMENTATION OF THE KEYED-HASH MESSAGE AUTHENTICATION CODE (HMAC) USING THE SHA-1 HASH FUNCTION,

A. Kakarountas, H. Mihail, A. Milidonis, C. Goutis, University of Patras, Patras, Greece.

In this paper an efficient implementation, in terms of performance, of the keyed-hash message authentication code (HMAC) using the SHA-1 hash function is presented. This mechanism is used for message authentication using a secret key. The proposed hardware implementation, which was described using VHDL, can be synthesized targeting a variety of FPGA and ASIC technologies. Simulation results, using commercial tools, verify the efficiency of the HMAC implementation in terms of speed and throughput. Special care has been taken so that the proposed implementation doesn't introduce extra design complexity; while in parallel functionality was kept to the required levels.

WB3.2

COMPARISON OF THE HARDWARE ARCHITECTURES AND FPGA IMPLEMENTATIONS OF STREAM CIPHERS,

M. Galanis, P. Kitsos, G. Kostopoulos, N. Sklavos, O. Koufopavlou, C. Goutis, University of Patras, Patras, Greece.

In this paper, the hardware implementations of five representative stream ciphers are compared in terms of performance and consumed area. The ciphers used for the comparison are the A5/1, W7, E0, RC4 and Helix. The first three ones have been used for the security part of well-known standards. The Helix cipher is a recently introduced fast, word oriented, stream cipher. W7 algorithm has been proposed as a more trustworthy solution for GSM, due to the security problems that occurred concerning A5/1 strength. The designs were coded using VHDL language. For the hardware implementation of the designs, an FPGA device was used. The implementation results illustrate the hardware performance of each cipher in terms of throughput-to-area ratio. This ratio equals to: 5.88 for the A5/1, 1.26 for the W7, 0.21 for the E0, 2.45 for the Helix and 0.86 for the RC4.

WB3.3

HIGH PERFORMANCE CRYPTOGRAPHIC ENGINE PANAMA:

HARDWARE IMPLEMENTATION, G. Selimis, P. Kitsos, O. Koufopavlou, University of Patras, Patras, Greece.

In this paper a hardware implementation of a dual operation cryptographic engine PANAMA is presented. The implementation of PANAMA algorithm can be used both as a hash function and a stream cipher. A basic characteristic of PANAMA is a high degree of parallelism which has as result high rates for the overall system throughput. An other profit of the PANAMA is that one only architecture supports two cryptographic operations – encryption/ decryption and data hashing. The proposed system operates in 96.5 MHz frequency with maximum data rate 24.7 Gbps. The proposed system outperforms previous any hash functions and stream ciphers implementations in terms of performance. Additional techniques can increase the achieved throughput about 90%.

WB3.4

BULK ENCRYPTION CRYPTO-PROCESSOR FOR SMART CARDS:

DESIGN AND IMPLEMENTATION, N. G. Sklavos, G. Selimis, O. Koufopavlou, University of Patras, Patras, Achaia, Greece.

The evolution of cipher has no practical impact, if it has only theoretical background. Every encryption algorithm should exploit as much as possible the conditions of the specific system without omitting the physical, area and timing limitations. The environment of smart card lacks of system resources but the commercial and economic transactions via smart cards demand the use of certificated and secure cryptographic methods. This fact requires new ways in design architectures for secure and reliable Smart Card systems. In this paper, a Crypto-Processor architecture and the VLSI implementation for smart cards bulk encryption is proposed. The proposed architecture achieves 30% area resources reduction and has throughput value much greater than the smart cards standards specify.

WC3: LOW NOISE AMPLIFIERS

Wednesday, December 15

Time: 14:00 – 15:40

Hall: Tabor

Chair: **I. Filanovsky**, University of Alberta, Canada

WC3.1

A DESIGN FLOW FOR INDUCTIVELY DEGENERATED LNA'S, D.

Guermendi, E. Franchi, A. Gnudi, University of Bologna, Bologna, Italy.

A design flow to explore the design parameters space of integrated inductively-degenerated Low Noise Amplifiers (LNA) under the constraint of matched input impedance is presented. It is based on standard circuit simulation tools and can be easily automated. The method is applied for the designing of a 5.5GHz 0.18um CMOS LNA with minimum noise figure (NF) for a fixed bias current. The measured NF of 2.6dB, with input reflection coefficient lower than -15dB at 5mA bias current, shows good agreement with simulations.

WC3.2

DESENSITIZED DESIGN OF MOS LOW NOISE AMPLIFIERS BY R_n

MINIMIZATION, *G. Banerjee, *D. Becher, *C. Hung, *K. Soumyanath, **D.

Allstot, *Intel Corporation, Hillsboro, OR, USA, **University of Washington, Seattle, WA, USA.

We show that the minimization of device R_n allows us to simultaneously approach noise and input match in CMOS LNA designs in a topology-independent fashion. The dependence of R_n on designer specifiable parameters is derived using a theoretical analysis of long channel (i.e., square law) devices. Experimental results are shown to confirm this dependence for short-channel devices. Using experimental data from a 0.18 um CMOS technology, we show that a low R_n design results in a $> 2x$ increase in the bandwidth over which an optimal noise figure can be obtained. The desensitization of the device with a low R_n provides a greater immunity to impedance mismatches, modeling errors and manufacturing variations.

WC3.3

A HIGH-SPEED CMOS OP-AMP DESIGN TECHNIQUE USING NEGATIVE

MILLER CAPACITANCE, B. Shem-Tov, M. Kozak, E. G. Friedman, University of Rochester, Rochester, NY, USA.

A method is presented in this paper for the design of high speed CMOS Operational Amplifiers (Op-Amp). The Op-Amp consists of an Operational

Transconductance Amplifier (OTA) followed by an output buffer. The OTA is compensated with a capacitor connected between the input and output of the buffer. An Op-Amp is designed in a 0.18 μm standard digital CMOS technology and exhibits 86 dB DC gain. The unity gain frequency and phase margin are 392 MHz and 73°, respectively, for a parallel combination of 2 pF and 1 k Ω load. As compared to the conventional approach, the proposed compensation method results in a 1.5 times increase in unity gain frequency and a 35° improvement in the phase margin under the same load condition.

WC3.4

ADAPTIVE ANALOG-TO-DIGITAL CONVERSION USING SELF-DITHERING IN DATA ACQUISITION SYSTEMS, *

***, **J. M. D. Dias Pereira, *P. S. Girao, **O. Postolache, Instituto de Telecomunicacoes, Lisbon, Portugal, **Escola Superior de Tecnologia, Setubal, Portugal.**

Sampling rate and resolution are two main competing interests in digital data acquisition systems design. High sampling rate data acquisition systems, usually based on flash converters, exhibits low-resolution, and high resolution systems, usually based on sigma-delta or dual-slope converters, are generally slow. However, a compromise can be obtained if digital signal processing techniques are used after analog-to-digital conversion. This paper presents a solution that can be used to optimize the performance of data acquisition systems based on analog-to-digital data acquisition boards. A dynamic self-adjusted sampling rate and dithering are proposed in order to improve signal-to-noise relation and measurement accuracy. Simulation and experimental results will be presented to evaluate digitizing system performance gains when the proposed solution is applied.

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