Introduction to Digital VLSI Design
מבוא לתכנון VLSI

Routing

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Routing :- Making real Point to Point connections. Metal is used to create wires and Vias for inter metal layer connections.
The Routing Problem

- **Apply it after floorplanning/placement**
- **Input:**
  - Netlist
  - Timing budget for, typically, critical nets
  - Locations of blocks and locations of pins
- **Output:**
  - Geometric layouts of all nets
- **Objective:**
  - Minimize the total wire length, the number of vias, or just completing all connections without increasing the chip area.
  - Each net meets its timing budget.
The Routing Constraints

- **Examples:**
  - Placement constraint
  - Number of routing layers
  - Delay constraint
  - Meet all geometrical constraints (design rules)
  - Physical/Electrical/Manufacturing constraints:
    - Crosstalk
    - Process variations, yield, or lithography issues?

*Two-layer routing*  
*Geometrical constraint*
Approaches for Routing

• **Sequential Approach:**
  - Route nets one at a time.
  - Order depends on factors like criticality, estimated wire length, and number of terminals.
  - When further routing of nets is not possible because some nets are blocked by nets routed earlier, apply ‘Rip-up and Reroute’ technique (or ‘Shove-aside’ technique).

• **Concurrent Approach:**
  - Consider all nets simultaneously, i.e., no ordering.
  - Can be formulated as integer programming.
Extraction and Timing Analysis

• After global routing and detailed routing, information of the nets can be extracted and delays can be analyzed.
• If some nets fail to meet their timing budget, detailed routing and/or global routing needs to be repeated.
How Routers Work

1. Divide Interconnection network in Net segments
2. Assign Net segments to regions or Channels
3. Identify Sequence for the nets to be routed
4. Create Actual Geometries and Join using VIAs (Size, Position and Layer for each net segment)
5. Identify Violations, rip off and Reroute

Global Route
Detail Route
Search & Repair
Routing

• Problem
  ▪ Given a placement, and a fixed number of metal layers, find a valid pattern of horizontal and vertical wires that connect the terminals of the nets
  ▪ Levels of abstraction:
    o Global routing
    o Detailed routing

• Objectives
  ▪ Cost components:
    o Area (channel width) – min congestion in prev levels helped
    o Wire delays – timing minimization in previous levels
    o Number of layers (less layers → less expensive)
    o Additional cost components: number of bends, vias
Routing Anatomy

Top view

3D view

Symbolic Layout

Metal layer 1
Via
Metal layer 2
Metal layer 3

Note: Colors used in this slide are not standard
Global vs. Detailed Routing

• **Global routing**
  - Input: detailed placement, with exact terminal locations
  - Determine “channel” (routing region) for each net
  - Objective: minimize area (congestion), and timing (approximate)

• **Detailed routing**
  - Input: channels and approximate routing from the global routing phase
  - Determine the exact route and layers for each net
  - Objective: valid routing, minimize area (congestion), meet timing constraints
  - Additional objectives: min via, power
Routing Environment

- **Routing regions**
  - **Channel**
    - Fixed height?
      - (→ fixed number of tracks)
    - Fixed terminals on top and bottom
    - More constrained problem: switchbox. Terminals on four sides fixed
  - **Area routing**
    - Wires can pass through any region not occupied by cells
      - (exception: over-the-cell routing)

- **Routing layers**
  - Could be pre-assigned (e.g., M1 horizontal, M2 vert.)
  - Different weights might be assigned to layers
Routing Environment

• Chip architecture
  § Full-custom:
    o No constraint on routing regions
  § Standard cell:
    o Variable channel height?
    o Feed-through cells connect channels
  § FPGA:
    o Fixed channel height
    o Limited switchbox connections
    o Prefabricated wire segments have different weights
Taxonomy of VLSI Routers

- **Routers**
  - **Global**
    - Graph Search
    - Steiner
    - Iterative
    - Maze
  - **Detailed**
    - Restricted
      - River
      - Switchbox
      - Channel
    - General Purpose
      - Maze
      - Line Probe
      - Line Expansion
  - **Specialized**
    - Power/Gnd
    - Clock
  - Hierarchical
  - Greedy
  - Left-Edge
Global Routing Approaches

• A combination of different approaches might be used in chip-level routing
  - Route simple nets (2-3 pins in local area) directly (e.g., L-shaped or Z-shaped)
  - Use a “close to optimal” Steiner Tree algorithms to route nets of intermediate length
  - Route remaining “big” nets using a maze router

• Ordering
  - Some ordering is chosen, if can route all, then done, otherwise:
  - Rip-up and Re-route
Steiner Tree Based Algorithms

- For multi-terminal nets.
- Find Steiner tree instead of shortest path.
- Construct a Steiner tree from the minimum spanning trees (MST)
Net Ordering

- In sequential approach, we need some **net ordering**.
- A bad net ordering will increase the total wire length, and may even prevent completion of routing for some circuits which are indeed routable.
After Global Routing: Detailed Routing

The routing regions are divided into channels and switchboxes.

So only need to consider the channel routing problem and the switchbox routing problem.
Channel Routing for Different Styles

- For Gate-array design, channel widths are fixed. The goal is to finish routing of all the nets.
- For Standard-cell and Full-custom design, channels are expandable. The goal is to route all nets using the minimum channel width.
- We will consider the case when the channels are expandable.
Routing Layer Models

1 layer

2 layers

3 layers

- VH model
- HV model
- VHV model
- HVH model

Layer 1
Layer 2
Layer 3
Via
FPGA Architecture - Layout

- **Island FPGAs**
  - Array of functional units
  - Horizontal and vertical routing channels connecting the functional units
  - Versatile switch boxes
  - Example: Xilinx, Altera

- **Row-based FPGAs**
  - Like standard cell design
  - Rows of logic blocks
  - Routing channels (fixed width) between rows of logic
  - Example: Actel FPGAs
FPGA Programmable Switch Elements

- **Used in connecting:**
  - The I/O of functional units to the wires
  - A horizontal wire to a vertical wire
  - Two wire segments to form a longer wire segment
Some Specific Routing Situations

Eco Route :-

a) To account for minor changes in design like:-
   Netlist change, buffer addition/resizing, gate addition/resizing etc.

b) Reroute partial routes and nets without routing.

c) Retains fully prerouted nets and pin-to-pin paths.
Routing Clocks

During CTS:-

RouteTypeName <routing type name A>
NonDefaultRule <non default rule name>
TopPreferredLayer 5
BottomPreferredLayer 4
...
END

RouteTypeName <routing type name B>
TopPreferredLayer 3
BottomPreferredLayer 2
...
END

AutoCTSRootPin clk_250
...
RouteType <routing type name A>
LeafRouteType <routing type name B>
RouteClnNet Yes
PostOpt YES
...
END

During Routing:-

a) Assign weight
b) Assign top and bottom routing layer
c) Assign extra spacing if possible
d) Use avoid detour
e) Route clock first if possible
Contd…

Timing Driven Routing

Router restricts the routing of Timing-critical nets.

Increase in Run time and number of violations.
Shielded routing is performed to protect noise-sensitive nets.

Nets are shielded using power or ground wires.