National Semiconductor

May 2001

CLC400
Fast Settling, Wideband Low Gain Monolithic Op Amp

General Description

The CLC400 is a high speed, fast setting operational amplifier designed for low gain applications. Constructed using a unique, proprietary design and an advanced complementary bipolar process, the CLC400 offers performance far beyond that normally offered by ordinary monolithic op amps. In addition, unlike many other high speed op amps the CLC400 offers both high performance and stability without the need for compensation circuitry — even at a gain of +1.

The fast 12ns settling to 0.05% and its ability to drive capacitive loads makes the CLC400 an ideal flash A/D driver. The wide bandwidth of 200MHz and the very linear phase ensure unsurpassed signal fidelity. Systems employing digital to analog converters also benefit from the use of the CLC400 — especially if linearity and drive levels are important to system performance.

The CLC400 provides a simple, high performance solution for video distribution and line driving applications. The 50mA output current and guaranteed specifications for 100Ω loads provide ample drive capability and assured performance.

The CLC400 is based on **National's** proprietary op amp topology that uses current feedback instead of the usual voltage feedback. This unique design has many advantages over conventional designs (such as settling time that is relatively independent of gain), yet it is used in basically the same way (see the gain equations in *Figure 1* and *Figure 2*). However, an understanding of the topology will aid in achieving the best performance. The following discussion will proceed for the non-inverting gain configuration with the inverting mode analysis being very similar.

Enhanced Solutions (Military/Aerospace)

SMD Number: 5962-89970

Space level versions also available.

For more information, visit http://www.national.com/mil

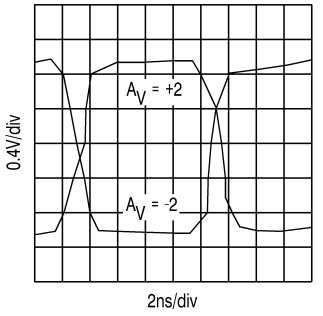
Features

- −3dB bandwidth of 200MHz
- 0.05% settling in 12ns
- Low power, 150mW
- Low distortion, −60dBc at 20MHz
- Stable without compensation
- Overload and short circuit protected
- ±1 to ±8 closed loop gain range

Applications

- Flash, precision A/D conversion
- Video distribution
- Line drivers
- D/A current-to-voltage conversion
- Photodiode, CCD preamps
- IF processors
- High speed communications

Pulse Response



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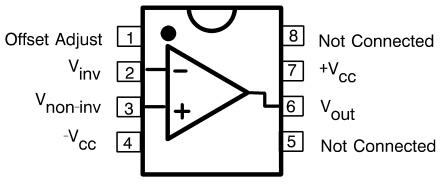
Connection Diagram



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Pinout
DIP & SOIC

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Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
8-pin plastic DIP	−40˚C to +85˚C	CLC400AJP	CLC400AJP	N08E
8-pin plastic SOIC	−40˚C to +85˚C	CLC400AJE	CLC400AJE	M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	±7V
I_{OUT} Output is short circuit protected to ground, but maximum reliability will be maintained if I_{OUT} does not exceed...	60mA
Common Mode Input Voltage	$\pm V_{CC}$
Differential Input Voltage	10V
Junction Temperature	+150˚C
Operating Temperature Range	−40˚C to +85˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Solder Duration (+300˚C)	10 sec
ESD rating (human body model)	500V

Operating Ratings

Thermal Resistance Package	(θ_{JC})	(θ_{JA})
MDIP	70˚C/W	125˚C/W
SOIC	65˚C/W	145˚C/W

Electrical Characteristics

A_V = +2, V_{CC} = ±5V, R_L = 100Ω, R_f = 250Ω; Unless Specified

Symbol	Parameter		Conditions	Typ	Max/Min Ratings (Note 2)			Units
Ambient Temperature			CLC400AJ	+25˚C	−40˚C	+25˚C	+85˚C	
Frequency Domain Response								
SSBW	-3dB Bandwidth		V_{OUT} <0.5V_{PP}	200	150	150	120	MHz
LSBW			V_{OUT}<5V_{PP}, A_V = +5	50	35	35	35	MHz
	Gain Flatness		V_{OUT}< 0.5V_{PP}					
GFPL	Peaking		<40MHz	0	0.4	0.3	0.4	dB
GFPH	Peaking		>40MHz	0	0.7	0.5	0.7	dB
GFR	Rolloff		<75MHz	0.6	1.0	1.0	1.3	dB
LPD	Linear Phase Deviation		to 75MHz	0.2	1.0	1.0	1.2	deg
Time Domain Response								
TRS	Rise and Fall Time		0.5V Step	1.6	2.4	2.4	2.4	ns
TRL			5V Step	6.5	10	10	10	ns
TSP	Settling Time to ±0.1%		2V Step	10	13	13	13	ns
TS	Settling Time to ±0.05%		2V Step	12	15	15	15	ns
OS	Overshoot		0.5V Step	0	15	10	10	%
SR	Slew Rate	A_V = +2		700	430	430	430	V/µs
SR1		A_V = −2		1600	–	–	–	V/µs
Distortion And Noise Response								
HD2	2nd Harmonic Distortion		2V_{PP},20MHz	−60	−40	−45	−45	dBc
HD3	3rd Harmonic Distortion		2V_{PP},20MHz	−60	−50	−50	−50	dBc
	Equivalent Input Noise							
SNF	Noise Floor		>1MHz	−157	−154	−154	−153	dBm (1Hz)
INV	Integrated Noise		1MHz to 200MHz	40	57	57	63	µV
Static, DC Performance								
VIO	Input Offset Voltage (Note 3)			2	±8.2	±5.0	±9.0	mV
DVIO	Average Temperature Coefficient			20	±40	–	±40	µV/˚C
IBN	Input Bias Current (Note 3)		Non-Inverting	10	±36	±20	±20	µA
DIBN	Average Temperature Coefficient			100	±200	–	±100	nA/˚C
IBI	Input Bias Current (Note 3)		Inverting	10	±36	±20	±30	µA
DIBI	Average Temperature Coefficient			50	±200	–	±100	nA/˚C
PSRR	Power Supply Rejection Ratio			50	45	45	45	dB
CMRR	Common Mode Rejection Ration			50	45	45	45	dB
ICC	Supply Current (Note 3)		No Load	15	23	23	23	mA

Electrical Characteristics (Continued)

A_V = +2, V_{CC} = ±5V, R_L = 100Ω, R_f = 250Ω; Unless Specified

Symbol	Parameter	Conditions	Typ	Max/Min Ratings (Note 2)			Units
Miscellaneous Performance							
RIN	Non Inverting Input	Resistance	200	>50	>100	>100	kΩ
CIN		Capacitance	0.5	<2.0	<2.0	<2.0	pF
RO	Output Impedance	At DC	0.1	<0.2	<0.2	<0.2	Ω
VO	Output Voltage Range	No Load	±3.5	>3.0	>3.2	>3.2	V
CMIR	Common Mode Input Range	For Rated Performance	±2.1	>1.2	>2.0	>2.0	V
IO	Output Current		±60	>35	>50	>50	mA

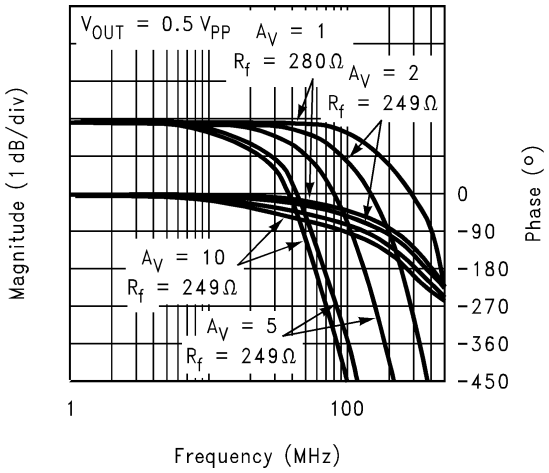
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Max/min ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Note 3: AJ-level: spec. is 100% tested at +25˚C, sample at 85˚C.

Typical Performance Characteristics (T_A = 25˚C, A_V = +2, V_{CC} = ±5V, R_L = 100Ω; Unless Specified).

Non-Inverting Frequency Response



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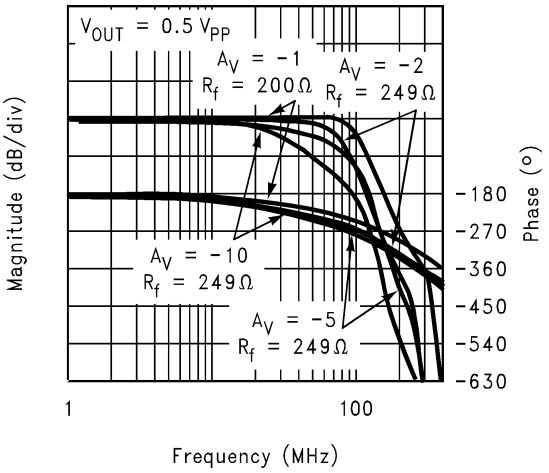
Inverting Frequency Response



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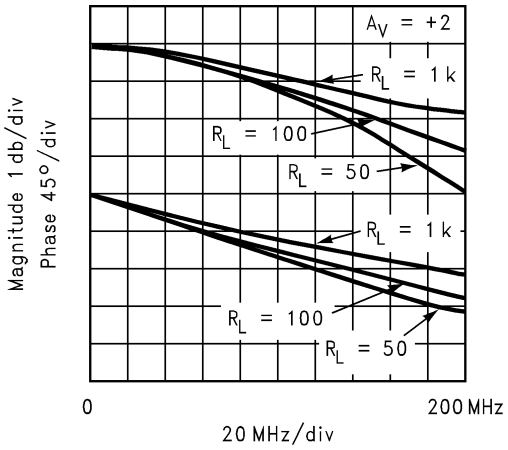
Frequency Response for Various R_LS



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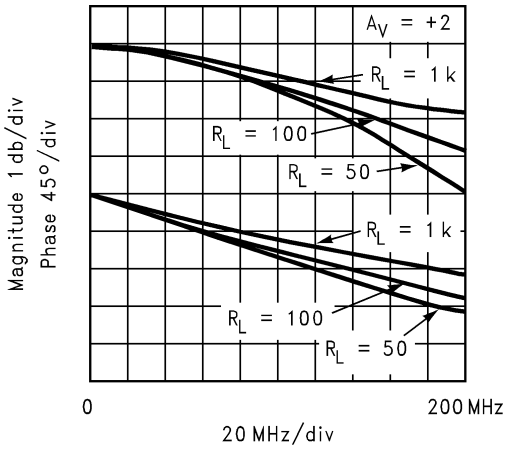
Frequency Response for Various R_LS



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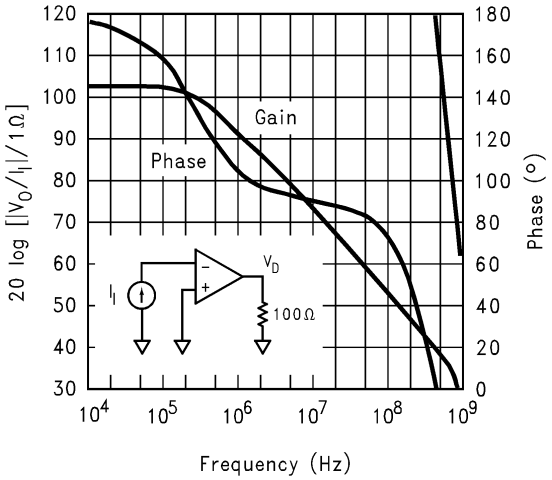
Typical Performance Characteristics (T_A = 25°C, A_V = +2, V_{CC} = ±5V, R_L = 100Ω; Unless Specified). (Continued)

Open-Loop Transimpedance Gain, Z(s)



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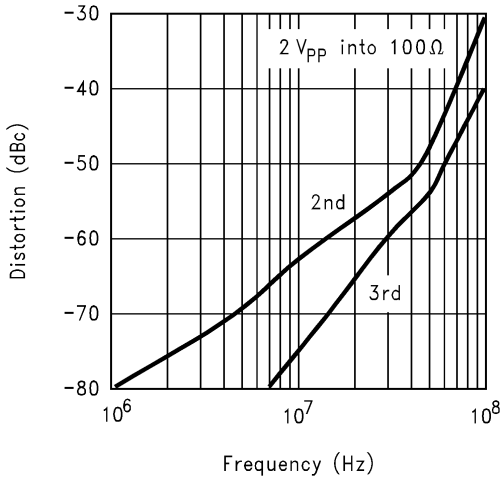
2nd and 3rd Harmonic Distortion



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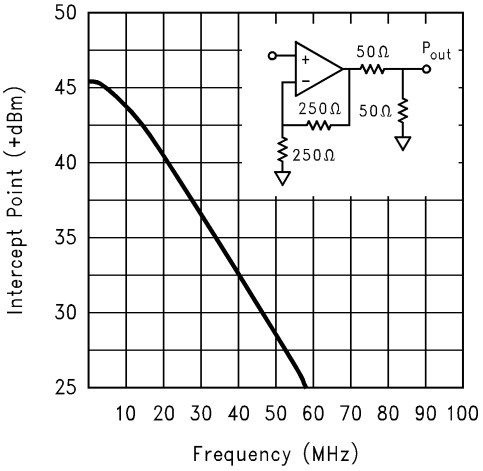
2-Tone, 3rd Order, Intermodulation Intercept



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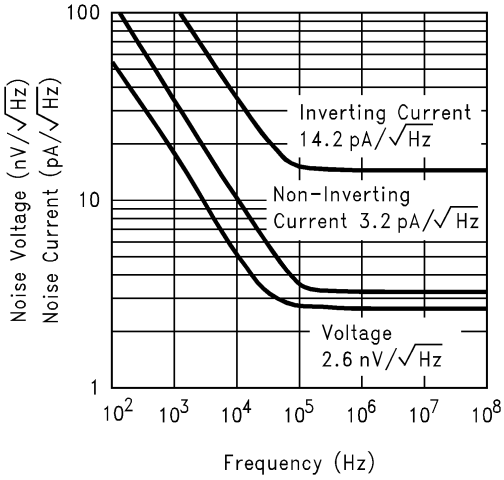
Equivalent Input Noise



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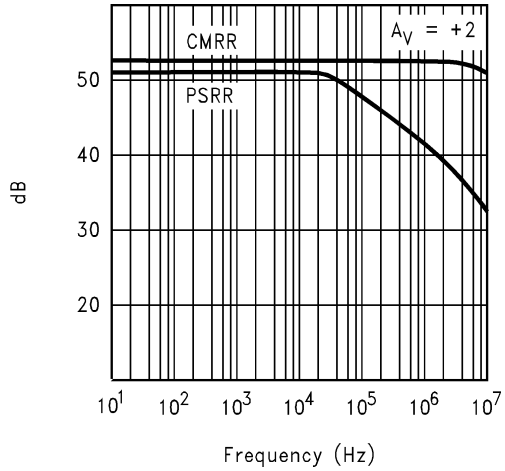
CMRR and PSRR



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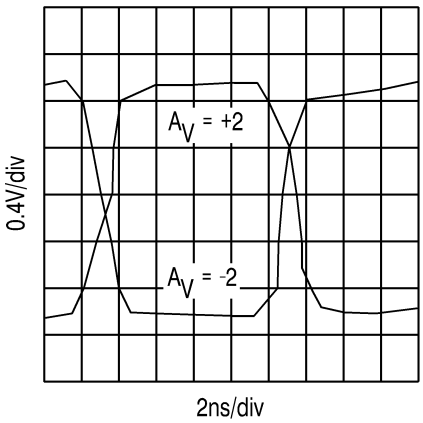
Pulse Response



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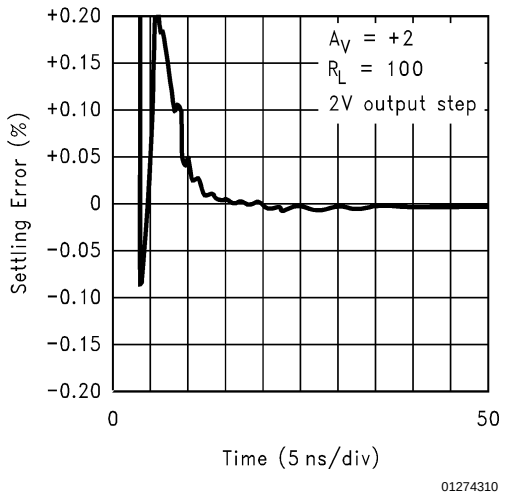
Typical Performance Characteristics (T_A = 25°C, A_V = +2, V_{CC} = ±5V, R_L = 100Ω; Unless Specified). (Continued)

Settling Time



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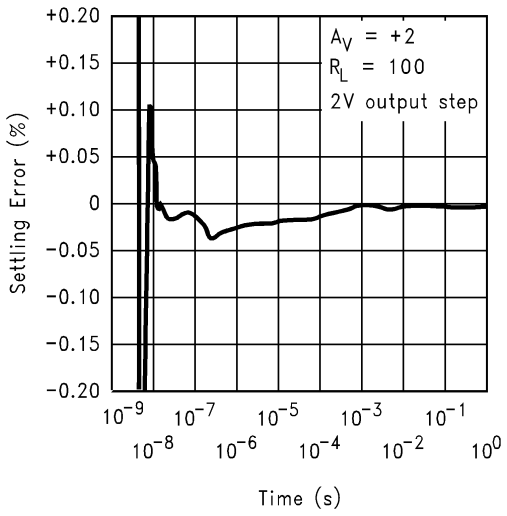
Long-Term Settling Time



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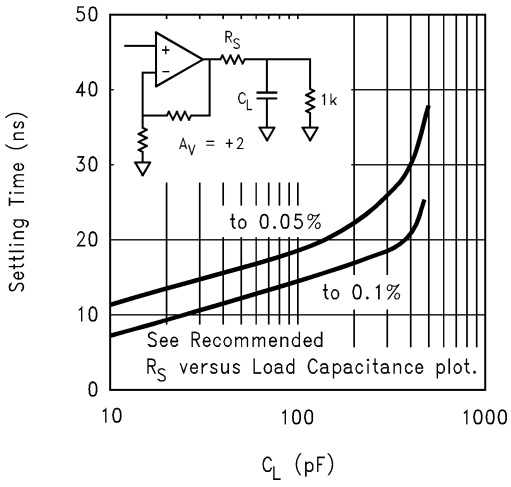
Settling Time vs. Load Capacitance



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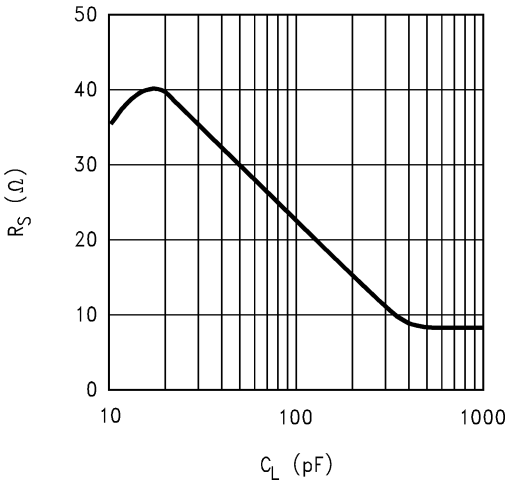
Recommended RS vs. Load Capacitance



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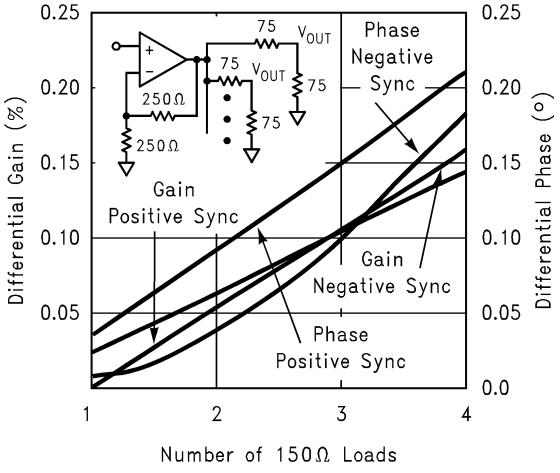
Differential Gain and Phase (4.43MHz)



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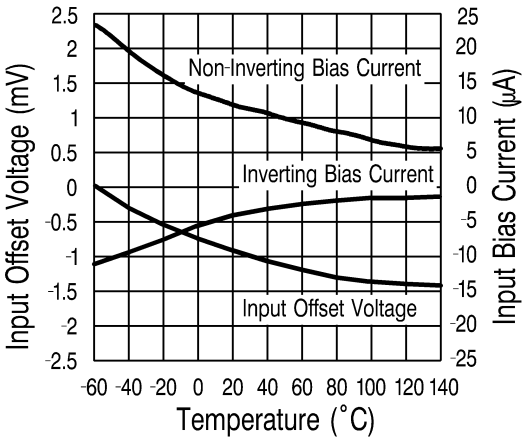
Typical DC Errors vs. Temperature



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Application Division

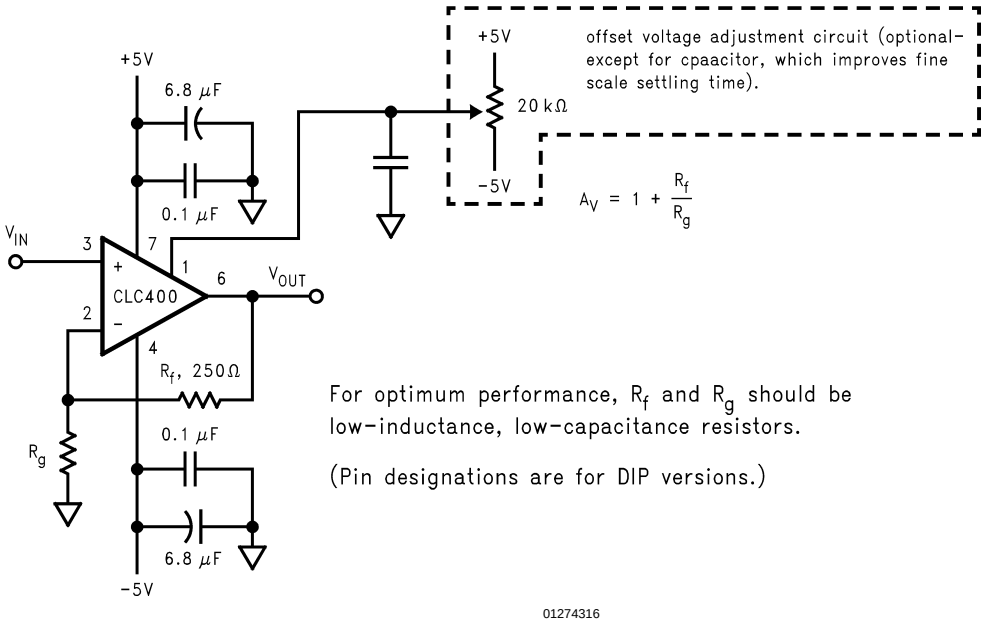


FIGURE 1. Recommended Non-Inverting Gain Circuit

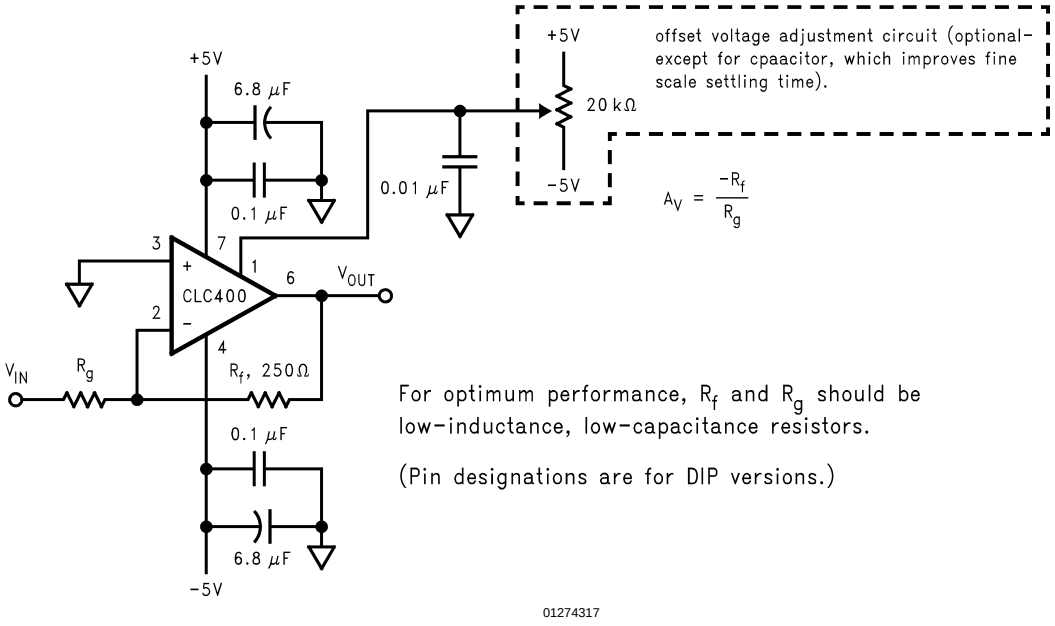


FIGURE 2. Recommended Inverting Gain Circuit

Understanding the Loop Gain

Referring to the equivalent circuit of *Figure 3*, any current flowing in the inverting input is amplified to a voltage at the output through the transimpedance gain shown on the plots. This Z(s) is analogous to the open-loop gain of a voltage feedback amplifier.

Application Division (Continued)

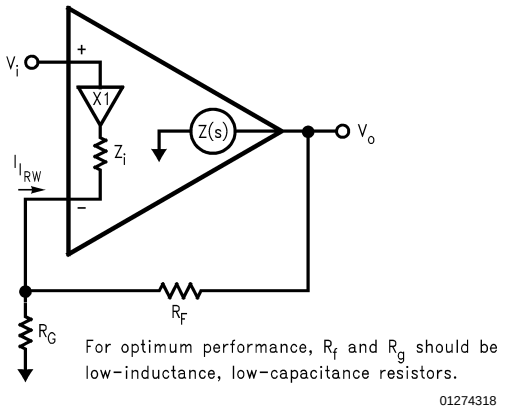


FIGURE 3. Current Feedback Topology

Developing the non-inverting frequency response for the topology of *Figure 3* yields:

Equation 1

$$\frac{V_o}{V_i} = \frac{1 + R_f / R_g}{1 - 1 / LG}$$

where LG is the loop gain defined by,

Equation 2

$$LG = \frac{Z(s)}{R_f} \times \frac{1}{1 + Z_i / (R_f \,||\, R_g)}$$

Equation 1 has a form identical to that for a voltage feedback amplifier with the differences occurring in the LG expression, Equation 2. For an idealized treatment, set Z_i=0 which results in a very simple LG = Z(s)/R_f (Derivation of the transfer function for the case where Z_i=0 is given in Application Note AN300-1). Using the Z(s) (open-loop transimpedance gain) plot shown on the previous page and dividing by the recommended R_f = 250Ω, yields a large loop gain at DC. As a result, Equation 1 shows that the closed-loop gain at DC is very close to (1+R_f/R_g).

At higher frequencies, the roll-off of Z(s) determines the closed-loop frequency response which, ideally, is dependent only on R_f. **The specifications reported on the previous pages are therefore valid only for the specified R = 250Ω.** Increasing R from 250 will decrease the loop gain and band width, while decreasing it will increase the loop gain possibly leading to inadequate phase margin and closed-loop peaking. Conversely, fixing R_f will hold the frequency response constant while the closed-loop gain can be adjusted using R_g.

The CLC400 departs from this idealized analysis to the extent that the inverting input impedance is finite. With the low quiescent power of the CLC400, Z = 50Ω leading to a drop in loop gain and bandwidth at high gain settlings, as given by Equation 2. The second term is Equation accounts for the division in feedback current that occurs between Z_i and R_f||R_g at the inverting node of the CLC400. This decrease in bandwidth can be circumvented as described in "Increasing Bandwidth at High Gains."

DC Accuracy and Noise

Since the two inputs for the CLC400 are quite dissimilar, the noise and offset error performance differs somewhat from that of a standard differential input amplifier. Specifically, the inverting input current noise is much larger than the non-inverting current noise. Also the two input bias currents are physically unrelated rendering bias current cancellation through matching of the inverting and non-inverting pin resistors ineffective.

In Equation 3, the output offset is the algebraic sum of the equivalent input voltage and current sources that influence DC operation. Output noise is determined similarly except that a root-sum-of-squares replaces the algebraic sum. $R_s$is the non-inverting pin resistance.

Equation 3

Output Offset V_o = ±IBN x R_S (1+ R_f/R_g) ±

VIO (1+ R_f/R_g) ±IBI x R_f

An important observation is that for fixed R_f, offsets as referred to the input improve as the gain is increased (divide all terms by 1+R_f/R_g). A similar result is obtained for noise where noise figure improves as a gain increases

Selecting Between the CLC400 or CLC401

The CLC400 is intended for gains of ±1 to ±8 while the CLC401 is designed for gains of ±7 to ±50. Optimum performance is achieved with a feedback resistor of 250Ω with the CLC400 and 1.5Ω with the CLC401- this distinction may be important in transimpedance applications such as D/A buffering. Although the CLC400 can be used at higher gains, the CLC401 will provide a wider bandwidth because loop gain losses due to finite Z_i are lower with the larger CLC401 feedback resistor as explained above. On the other hand, the lower recommended feedback resistance of the CLC400 minimizes the output errors due to inverting input noise and bias currents.

Increasing Bandwidth At High Gains

Bandwidth may be increased at high closed-loop gains by adjusting R_f and R_g to make up for the losses in loop gain that occur at these high gain settlings due to current division at the inverting input. An approximate relationship may be obtained by holding the LG expression constant as the gain is changed from the design point used in the specifications (that is, R_f = 250Ω and R_g = 250Ω). For the CLC400 this gives,

Equation 4

$$R_f = 350 - 50A_V \text{ and } R_g = \frac{350 - 50A_V}{A_V - 1}$$

where A_V is the non-inverting gain. Note that with A_V = +2 we get the specified R_f = 250Ω, while at higher gains, a lower value gives stable performance with improved bandwidth.

Capacitive Feedback

Capacitive feedback should not be used with the CLC400 because of the potential for loop instability. See Application Note OA-7 for active filter realizations with the CLC400.

Offset Adjustment Pin

Pin 1 can be connected to a potentiometer as shown in*Figure 1* and used to adjust the input offset of the CLC400. Full

range adjustment of ±5V on pin 1 will yield a ±10mV input offset adjustment range. Pin 1 should always be bypassed to ground with a ceramic capacitor located close to the package for best settling performance.

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

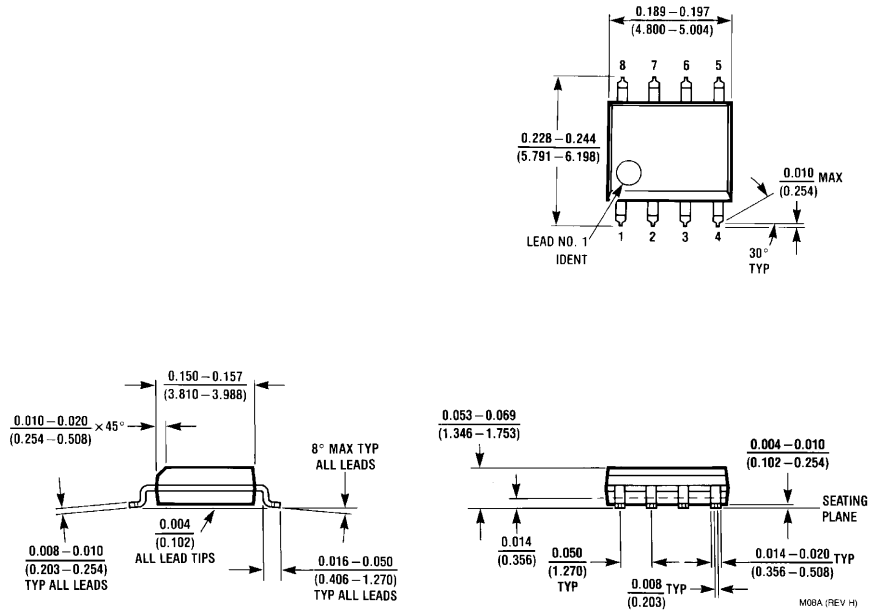
Parasitic or load capacitance directly on the output will introduce additional phase shift in the loop degrading the loop phase margin and leading to frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The graphs on the preceding page illustrate the required resistor value and resulting performance vs. capacitance.

Precision buffed resistors (PRP8351 series from Precision Resistive Products) with low parasitic reactances were used to develop the data sheet specifications. Precision carbon composition resistors will also yield excellent results. Standard spirally-trimmed RN55D metal film resistors will work with a slight decrease in bandwidth due to their reactive nature at high frequencies.

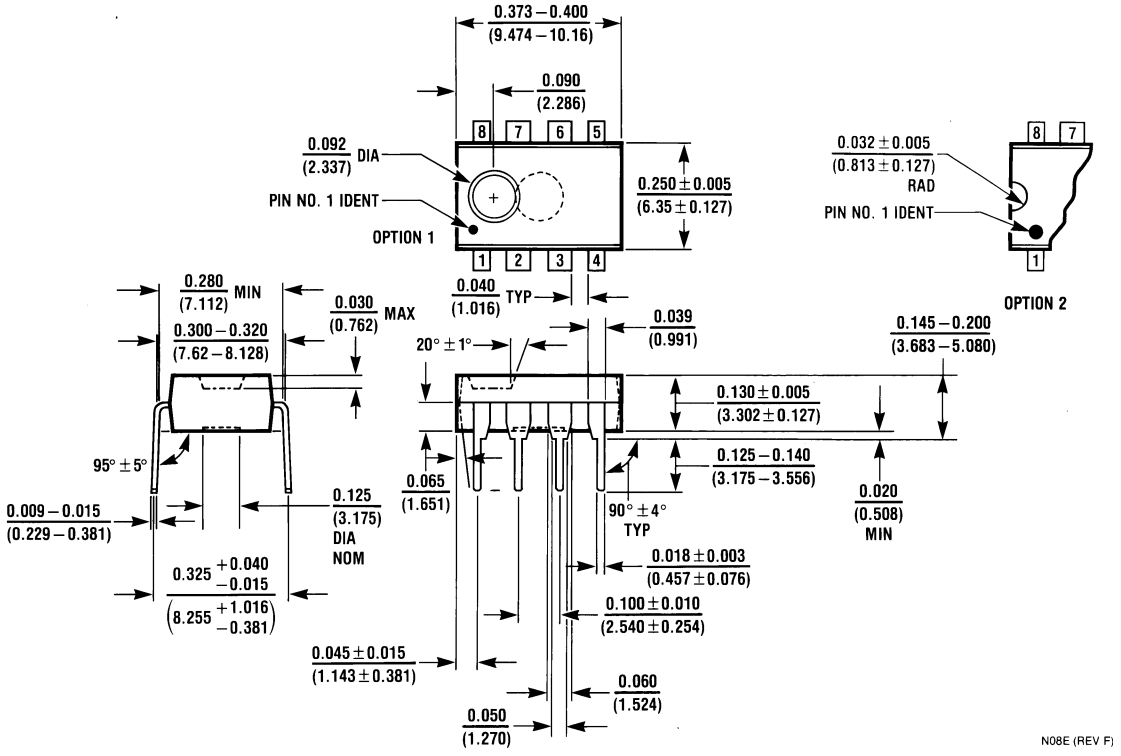
Evaluation PC boards (part no. 730013 for through-hole and 730027 for SOIC) for the CLC400 are available.

Physical Dimensions inches (millimeters)

unless otherwise noted



8-Pin SOIC
NS Package Number M08A



8-Pin MDIP
NS Package Number N08E

Notes

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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