

CMOS CURRENT/VOLTAGE MODE WINNER-TAKE-ALL CIRCUIT WITH SPATIAL FILTERING

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ABSTRACT

A CMOS Current/Voltage mode winner-take-all circuit (WTA) with spatial filtering for image processing applications is presented. This WTA circuit has a unique ability of spatial filtering that allows removal of the background from the image and is suitable for integration with CMOS Active Pixel Sensors. In this circuit, image intensity has been chosen for the input saliency map. The removal process is performed by zeroing the values of the image background intensity levels and transferring the new saliency map to a standard WTA circuit, so only the potential objects of interest are compared by the WTA.

Two circuits, current mode and voltage mode WTA circuits with filtering, have been implemented in 0.5 μm submicron CMOS technology. Their operation is discussed and simulation results are reported.

1. INTRODUCTION

Since Active Pixel Sensors are fabricated in a commonly used CMOS process, a sensor with integrated "intelligence" could be designed [1]. This kind of the sensor would be very useful in many scientific, commercial and consumer applications where spatial acquisition and tracking of the brightest object is sought. This includes star tracking, laser communication and many other applications. One task, critical for further development of these applications is the process of selecting an object and maintaining attention on it. Object selection that produces an output, which represents a single object of interest, can be accomplished using a winner-take-all (WTA) circuit. The function of the WTA is to accept the input signals from the APS, compare their values (the brightest pixel is accepted by the WTA as the largest signal), and assign a high (or low) distinct digital value to the brightest pixel. This distinct digital value corresponds to the largest input, while all other digital outputs are set to a low (or high) output value.

Many WTA circuit implementations have been proposed in the literature [2-7]. A current-mode MOS implementation of the WTA function was first introduced by Lazzaro [2]. Later, this circuit has been modified by Starzyk and Fang [3] by improving resolution and speed performance. In 1995 DeWeerth and Morris have added distributed hysteresis using a resistive network [4]. At the same time, additional works on voltage mode WTA circuit based on Lazzaro's circuit were presented [5,6]. In 1995 this circuit has been modified with feedback and inhibition by Wilson [5] and later, in 1999, by Kalim and Wilson [6]. Another work was proposed by Donckers, Dualibe and Verleysen [7]. The performances of all these circuits can be measured in terms of speed, accuracy, delay and power consumption. Most of these

circuits can be integrated with APS sensors. Some of them were designed specially for image processing, in which inputs are not stationary [4,9,10,11]. In these circuits the excitation and inhibition control the strategy for shifts of attention from one position to the next. Most of works describe a one-dimensional, n -element array of WTA. Others, for example [8], discuss 2D arrays. A further work of [12] discusses the elimination of the matching problem in such a circuit. As mentioned above, the regular WTA circuit chooses a winner from a group of input signals. So, when it is used for object selection, a problem can occur when the object of interest disappears from the processed image. In this case the WTA will compare the input voltages that are represented as intensity levels of image background. Hence a necessity of background filtering exists.

A technique for replacing values of low image intensity levels with zero (thresholding) was proposed in [10]. In this circuit the signal is compared against a globally set threshold, above which pixels qualify as object pixels. The disadvantage of this kind of filtering is that it is necessary to choose the value of this threshold in advance and in the case where the background is sufficiently bright (above the chosen threshold), the circuit will not be able to cope with the task. The worst case is if the object of the interest disappears from the processed image and the background is bright.

This paper proposes a new technique for background filtering. The filter circuit connects between the APS outputs and the regular WTA circuit inputs. It makes it possible to turn our attention to the fact that the object is not present in the image, and if it is present, it can improve the resolution of a regular WTA. The advantages of this circuit are that it is not necessary to know the values of the background voltages in advance, and it also is not necessary to choose the threshold value.

Two kinds of simple WTA circuits were chosen for implementation: 1. A CMOS current mode Winner-take-all circuit with local hysteresis after [3], 2. A Low power voltage mode Winner-take-all circuit after [7]. The reason for these choices is the simplicity of integration of these circuits with the filter. In principle, it is possible to connect the filter to any kind of WTA.

Section 2 describes the system architecture that was implemented to test the WTA circuits with spatial filtering. The specific circuits are described in Section 3. Section 4 describes the performance of these circuits including simulation results. Section 5 concludes the paper.

2. SYSTEM ARCHITECTURE

The system discussed in this paper is a one-dimensional, 8-element array of a current/ voltage mode WTA selection with spatial filtering, that can be easily enlarged to an n -element one-dimension or to an $n \times n$ 2D array. The system includes (1) An Active Pixel Sensor, (2) A Subtraction function (CDS - correlated

double sampling) implementation, (3) Spatial filtering, (4) A Winner-take-all selection circuit. The first and the second elements (APS and CDS) are not implemented in this test chip. The process of phototransduction in APS is performed in two stages: (1) The Reset stage (the charging of a capacitor to a reset voltage) (2) The Signal stage (the discharging of the capacitor through a constant integration time). Following this stage, we receive a low analog signal voltage for a bright pixel and a high signal voltage for a background pixel. The inputs to the filtering computation are voltages after the CDS. As a result, the brightest pixel is represented as the largest input voltage to filter.

The principle of the filter operation is to compare the differential output of each sensor to the average value of outputs from all sensors of the array plus an epsilon value. The result of this comparison is that if the CDS output of the specific sensor is lower, it is replaced by a zero value (ground in the case of a voltage mode WTA and zero current in the current mode WTA). In addition, the filter can point out that in all comparisons the CDS outputs were lower than the average plus an epsilon value. In this case we can conclude that only the background is present in the image.

The chip was designed to enable switching between the current and the voltage modes of the WTA operation.

3. CIRCUITS DESCRIPTION

3.1 The circuits block diagram

Fig.1 (a) and (b) show the block diagrams of the current and voltage mode WTA circuits with spatial filtering. The principle of operation is similar in both: the filter causes a replacement of the low background input value with ground, before it enters to the WTA. The difference is that in the current mode WTA there is an additional stage of V-I converting before the WTA.

As mentioned above, the APS and the CDS are not implemented in this test chip. The Unity Gain Amplifier is not implemented here either. The reason for mentioning the UGA is its importance in this specific circuit. The values of all differential voltages that are produced by the CDS are stored on capacitors. These voltages are converted into currents. The input resistance of the voltage to current converting circuit (V-I) is finite and not large, so the stored voltage can lose its value because of the leakage current into the V-I circuit. A UGA with approximately infinite input resistance solves this problem.

After the voltage is converted to current, the next stage is to calculate the average current of all pixels and add to it the epsilon value. Here, our assumption is that any object sensor is brighter than the background at least by epsilon. The epsilon value can be controlled in the average computation unit by an analog parameter.

The next stage is to compare the CDS ϵ output from every sensor with the average plus an epsilon value. If the results of all comparisons are '0', it means the object of interest disappears from the processed image. In this case the OR output will indicate that and all outputs of WTA will be '0'. If the result of any comparison will be '1', the output of the OR will be '1', and as mentioned in previous sections, the intensity level of this pixel will be transferred to the WTA (in voltage mode (a) it will be voltage and in the current mode (b) it will be current). The output of the WTA computation is '1' if the pixel is a winner, otherwise it will be '0'.

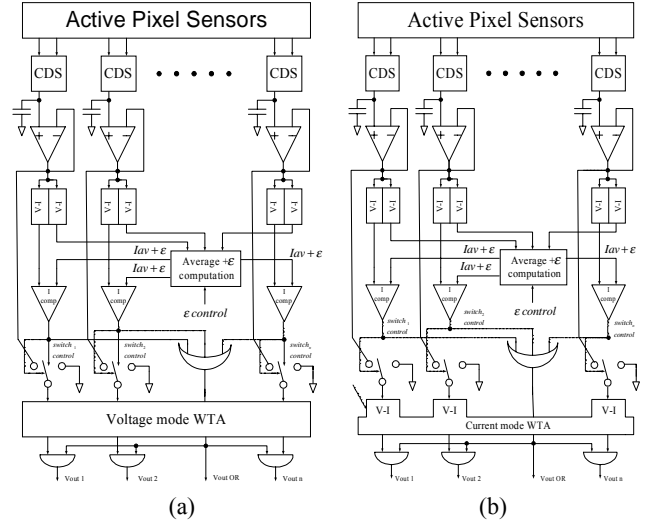


Fig 1. Block diagram of (a) current and (b) voltage winner-take-all circuits with spatial filtering.

3.2 V to I conversion circuits

Fig 2 (a) and (b) show the schemes of V to I circuits. The difference between the two is that the first one (a) is designed to pull the current and the second (b) pushes out the current.

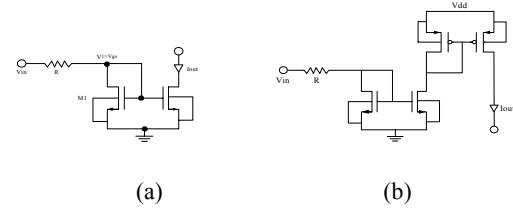


Fig 2. V to I conversion circuits: (a) current pull configuration (b) current push configuration

The circuits have a very simple structure and high operation speed. The reason for using input resistors instead of transistors is the range of the input voltages. The range of the input, which comes from the CDS circuit, is from 0V to 3.3V (from ground to Vdd), so if we want to operate the transistor in the linear zone, we need to supply the gate at least with $V_{dd} + V_t$. From simulation we can see that really we need 5.5V for optimal mode of operation. In this design the problem of resistor mismatch is not critical. All resistors have the same resistance value. We need high accuracy in the resistors value only when two input voltages are very close one to the other. The mismatch is less than 2% when the input voltages of all V-I's are the same. The mismatching increases with voltage difference increase. However, in this case the accuracy is less important.

This design characteristic of the circuits is not uniform in all input range. If $V_{in} < V_t$ then I_{out} dependence upon V_{in} is exponential, in other words, the circuit filters the small input voltages. This is an advantage for the global idea of the filter. If the range where $V_{in} > V_t$, I_{out} dependence upon V_{in} is approximately linear. It can be easily proved that for $V_{in} \gg V_t$:

$$(3.1) \quad I_{rr} = \frac{1}{2} k \frac{W}{l} (V_{gs} - V_t)^2, \text{ if } R_{rr} \gg R \Rightarrow V_{gs} = V_i \gg V_t$$

$$(3.2) R_{M1} = \left(\frac{dI}{dV_{gs}} \right)^{-1} = \frac{1}{k \frac{w}{l} (V_{gs} - V_t)} = \frac{l}{kwV_{gs}} = \frac{a}{V_t}$$

$$(3.3) V_1 = \frac{V_{in} R_{M1}}{R + R_{M1}} = \frac{V_{in} a}{R V_t + a}, \text{ if } R \approx a \text{ then}$$

$$(3.4) V_1^2 + V_1 = V_{in}, V_1 \gg 1 \Rightarrow V_1^2 \approx V_{in}$$

$$(3.5) V_1 \approx \sqrt{V_{in}}$$

$$(3.6) I_{ir} = \frac{1}{2} k \frac{w}{l} (V_1 - V_t)^2 = \frac{1}{2} k \frac{w}{l} (V_1)^2 = \frac{1}{2} k \frac{w}{l} (\sqrt{V_{in}})^2$$

$$(3.7) I_{ir} = I = \text{const} \cdot V_{in}$$

If $V_t < V_{in} \ll V_{dd}$ the proof is more complex, but it can be seen from the solution by MATLAB and Cadence Spectra simulation (Fig.5), that for $V_{in} > V_t + 400\text{mV}$ the dependence is still approximately linear (the dependence changes approximately exponential to approximately linear in this range).

3.3 Average+ε computation and current comparator circuits

Fig 3 (a) shows the scheme of the Average + ε computation circuit. Its inputs are the outputs from the V-I converting circuit and the drain of the ε control transistor (M1). The value of $w/2l$ of M2 is $n \cdot w/l$, when w/l is relates to M_{a1} - $M_{a,n}$ transistors. If the ε control input is zero, then the outputs of the circuit are the average current of the n inputs. We can add the ε value to this average by increasing the δ control value.

Fig 3 (b) shows the scheme of the current comparator circuit. It has a very simple structure and there are two inverters in the output in order to improve its performance.

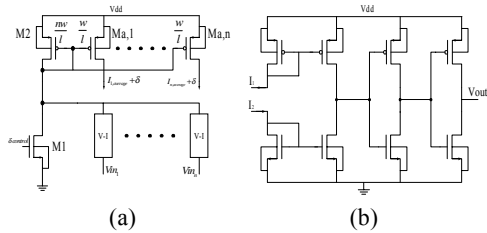


Fig 3. (a) Average+ε computation and (b) current comparator circuits.

3.4 Voltage and current mode WTA circuits

Fig 4 (a) shows the scheme of a single cell of a voltage mode winner-take-all circuit [7].

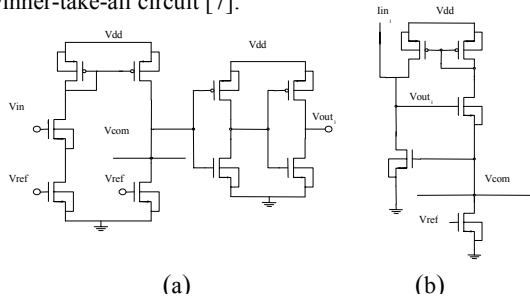


Fig 4. (a) Voltage and (b) current mode winner-take-all circuits.

It has a very simple architecture, high speed of operation and low power. The line V_{com} connects between cells and it is common to all of them. Fig 4 (b) shows the scheme of a single cell of the chosen current mode WTA [3]. This kind of circuit has a local hysteresis that is allowed by the current mirror. The full circuit description can be found in [7] for (a) and in [3] for (b).

4. PERFORMANCE AND SIMULATIONS

A circuit having 8 cells was designed and fabricated in the 0.5μm, 3.3V, n-well, 3-metal, CMOS, HP technology process supported by MOSIS. The test chip consists of 8 cells. The width of each cell is 14 λ, thus suitable to the pitch of one active pixel sensor.

The circuits were simulated with the SPECTRA Cadence simulator using HP 0.5μm CMOS process parameters. The supply voltage is 3.3V.

V-I conversion circuit: Fig. 5 shows the response of V-I converting circuit with $R=5\text{Kohm}$. The input is voltage that ranges from 0V to 3.3V. The output is the measured current. It can be seen from the simulation that the characteristic of the design that it fits the theory (section 3.2).

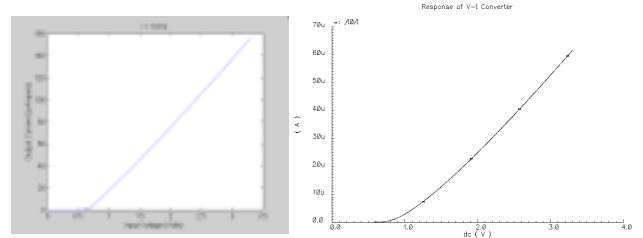


Fig 5. (a) Matlab solution for V-I characteristic, (b) Cadence Spectra simulated response of V-I converting circuit with $R=5\text{Kohm}$.

Filter simulated results: Two sets of simulations were carried out to determine the properties of the filter: 1. Simulation for a low level background 2. Simulation for a high level background. The reason for this kind of simulations is to check the ability of the circuit to filter background regardless its level. These following input voltages were used in the first simulation: (a) the set of voltages that represent a low background: $V_{in1}=0.4\text{V}$, $V_{in2}=0.5\text{V}$, $V_{in5}=0.6\text{V}$, $V_{in6}=0.6\text{V}$, $V_{in7}=0.7\text{V}$, $V_{in8}=0.8\text{V}$, (b) an input that represent the object of interest: $V_{in4}=1.5\text{V}$, (c) an input that ranges from 0V to 3.3V – represent the background in the case of a low value and the object in the case of a high value: V_{in3} . Fig 6(a) and Fig 6(b) show the response of the filter to this input vector. It can be see, that the control signal of cell 4 (the output of the filter that corresponds to V_{in4}) is high, because $V_4 > V_{\text{average}+\epsilon} \Rightarrow (I_4 > I_{\text{average}+\epsilon})$. The control signal of cell 3 is low for $V_{in3} < 0.89\text{V}$ and high for $V_{in3} > 0.89\text{V}$. This value represents the $V_{\text{average}+\epsilon}$ when $V_{in3}=0.89\text{V}$. Here, the ε control input is 1V. As mentioned before we can change the ε value by changing the ε control voltage. The set of inputs in the second simulation is: (a) a set of voltages that represent a low background: $V_{in1}=1.2\text{V}$, $V_{in2}=1.3\text{V}$, $V_{in5}=1.4\text{V}$, $V_{in6}=1.45\text{V}$, $V_{in7}=1.5\text{V}$, $V_{in8}=1.6\text{V}$, (b) an input that represents the object of interest: $V_{in4}=2.2\text{V}$, (c) an input that ranges from 0V to 3.3V: V_{in3} . In this case the background is high, and the control

signal of cell 3 is low for $V_{in3} < 1.7V$ and high for $V_{in3} > 1.7V$. From this simulations we can see that the filter output is not dependent on the background value.

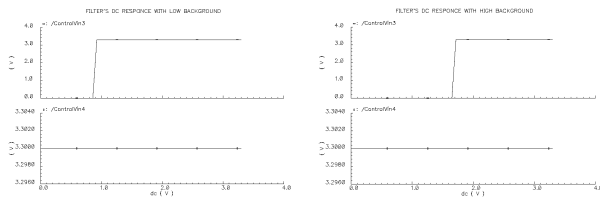


Fig 6. Filter response for the case of (a) low background, (b) high background.

Table 1 summarizes the main characteristics of the circuit. Note that the simulation takes parasitic capacitances into account. Filter delay is defined as the time interval between the circuit input voltage step and the input voltage step of the WTA .

Filter circuit	
Supply voltage	3.3V
Power consumption F=25KHz	58.2 uW/cell (typical) 948 uW/cell (max)
Delay	8 nsec (typical) 46 nsec (max)
Delay (in → OR output)	7 nsec (typical)

Table 1: Filter performance.

Note, that the max power is simulated in the case that all inputs are 3.3V.

Voltage and current mode WTA circuits with spatial filter: Table 2 summarizes the main characteristics of voltage and current mode WTA circuits with the filter.

	Voltage mode WTA+filter	Current mode WTA +filter
Supply voltage	3.3V	3.3V
Power consumption F=25KHz	75.2 uW/cell (typical) 965 uW/cell (max)	59 uW/cell (typical) 949 uW/cell (max)
Delay	350 nsec (typical)	56 nsec (typical)
Precision	40mV	1%

Table 2 WTA circuits with filtering characteristics.

5. CONCLUSIONS

System description, circuit design and simulation results of voltage/current mode winner-take-all circuits with spatial filtering have been presented. A prototype chip is being fabricated in a $0.5\mu m$ sub μm HP process. It operates of a single 3.3V supply and dissipates $75.2\mu W$ (typical for voltage mode of operation) at 25kHz. The circuit has a unique ability for spatial filtering that allows removal of the background from the image

and is suitable for integration with CMOS Active Pixel Sensors. Extensive simulations reveal the ability of the circuit to filter the background independent of its value. The proposed filter has a very simple structure and is suitable for integration with any kind of voltage or current mode winner-take-all circuits. The next stage is integration of the filter with more complex WTA circuits (after [9],[10], [11] for example) that are more suitable for image processings and widening the system to be of 2 dimensions.

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REFERENCES

- [1] O. Yadid-Pecht, E. R. Fossum, C. Mead, "APS image sensors with a winner-take-all (WTA) mode of operation", JPL/Caltech New Technology Report, NPO 20212.
- [2] J.Lazzaro., S.Ryckebusch, M.A. Mahowald, and C.A. Mead, "Winner-take-all networks of $O(n)$ complexity", 1:703-711, ed. D.S.Touretzky, Morgan Kaufmann, San Mateo, CA, 1989.
- [3] J.A.Startzyk and X.Fang, "CMOS Current mode Winner-take-all circuit with both excitatory and inhibitory feedback", Electronics Letters, 13th May 1993, Vol.29, No.10.
- [4] S.P.DeWeerth and T.G.Morris, "CMOS current mode winner-take-all circuit with distributed hysteresis", Electronics Letters, 22nd June 1995, Vol.31, No.13.
- [5] D.M.Wilson and S.P.DeWeerth, "Winning Isn't Everything", ISCAS'95, Seattle, Washington, pp.105-108, 1995.
- [6] R.Kalim and D.M.Wilson, "Semi-parallel rank-order filtering in analog VLSI", ISCAS'99. IEEE, Piscataway, NJ, USA; 1999; p.232-5, vol.2.
- [7] N. Donckers, C. Dualibe, M. Verleysen, "Design of Complementary Low-Power CMOS Architectures for Looser-take-all and Winner-take-all", Proceeding of the Seventh International Conference on Microelectronics for Neural, Fuzzy and Bio-Inspired Systems. IEEE Comput. Soc, Los Alamitos, CA, USA; 1999; xv+426 pp. P360-5
- [8] Z.Kalayjian, J.Waskiewicz, D.Yochelson, A.G.Andreou, "Asynchronous sampling of 2D arrays using winner-takes-all arbitration", ISCAS 96, IEEE, NY, USA; 1996; vol.3, p.393-6
- [9] T.G.Morris and S.P.Deweerth, "Analog VLSI Excitatory Feedback Circuits for Attentional Shifts and Tracking", Analog Integrated Circuits and Signal Processing, 1997, vol. 13, p. 79-91.
- [10] T.G.Morris, T. K.Horiuchi, and P.DeWeerth, "Object-Based Selection Within an Analog Visual Attention System", IEEE Transactions on circuits and systems-11, Analog and Digital Signal processing, vol.45, no.12, December 1998.
- [11] T.G.Moris and S. P.DeWeerth, "A Smart-Scanning Analog VLSI Visual-Attention System", Analog Integrated Circuits and Signal Processing, vol.21, p.67-78, 1999.
- [12] T.Serrano-Gotarredona and B. Linares-Barranco, "A High-Precision-Mode WTA-MAX Circuit with Multichip Capability", IEEE Journal of Solid-State Circuits, Vol. 33, No. 2, February 1998.