

In-Pixel Autoexposure CMOS APS

Orly Yadid-Pecht and Alexander Belenky

Abstract—A CMOS active pixel sensor (APS) with in-pixel autoexposure and a wide dynamic-range linear output is described. The chip features a unique architecture enabling a customized number of additional bits per pixel per readout, with minimal effect on the sensor spatial or temporal resolution. By utilizing multiple readouts via real-time feedback, each pixel in the field of view can automatically set an independent exposure time, according to its illumination. A customized, large increase in the dynamic range can be achieved and a scene containing both bright and dark regions can be captured. A prototype of 64×64 pixels has been fabricated using 1-poly 3-metal CMOS $0.5 \mu\text{m}$ n-well process available through MOSIS. Power dissipation is 3.7 mW at $V_{DD} = 5 \text{ V}$. The special functions have been verified experimentally, and an increase of 2 bits over the inherent dynamic range captured is shown.

Index Terms—Active pixel sensor (APS), CMOS imagers, column parallel architecture, dynamic range, image sensor, integration time, VLSI.

I. INTRODUCTION

SCENES imaged with electronic cameras can have a wide range of illumination depending on lighting conditions. Scene illuminations range from 10^{-3} lux for night vision to 10^5 lux for bright sunlight, and higher levels for direct viewing of other light sources such as oncoming headlights. However, typical charge-coupled devices (CCDs) and CMOS active pixel sensors (APSs) have a dynamic range of 65–75 dB. Previously suggested solutions for widening the dynamic range in CCD and APS sensors have been suggested. An extensive review of previous solutions can be found in [1].

Since this reported review, recent works continue research different ways of control of integration time for achieving a wide dynamic range. Both in CMD and CMOS, it has already been shown that an ultra wide dynamic range using two samples per frame could be achieved [2]–[4]. However, this will work well if the illumination levels are suited to one of the two integration times. If the illumination ranges somewhere in between, an accurate reading will not result. Multiple outputs could be read for different integration times. Yet, an additional frame memory for each extra reading is required, and also some synchronization process needs to be done since the readings will be set apart in their starting point.

A different architecture, achieving a wide dynamic range via more than two samples was lately suggested [5]. It requires, however, a large pixel area and in that proposal, the extra circuitry was divided between four neighboring pixels. Another sensor achieving a wide dynamic range was also proposed lately [6]. It requires, though, nonstandard CMOS technology

and a larger pixel area. In addition, three recent works proposed working along the frequency modulation approach, implemented in the pixel [7]–[9]. The first used the address event approach while the second utilizes in-pixel sigma-delta ADC, both of which require a high payment in fill factor. The third enables reset of a pixel, if a threshold is exceeded, to eliminate motion blur or saturation. Currently, the “frequency” is limited and normalization occurs outside the chip, but it has the potential of detecting very small changes accumulating long enough to pass a threshold. Pixel size is still problematic in these solutions.

The basic idea of this brief was presented in the ISSCC 01 conference [10]; a more detailed explanation is given here. We report an APS with in-pixel autoexposure and a wide dynamic-range linear output where minimum area above the basic APS transistors is required in the pixel, and with minimal effect on temporal resolution, yet achieving this additional dynamic range enhancement.

II. CHIP ARCHITECTURE

The architecture of our proposed approach is shown in Fig. 1.

As in a traditional rolling shutter APS, our imager is constructed of a two-dimensional (2-D) pixel array, here of 64 columns and 64 rows, with random pixel ability, fabricated on a semiconductor substrate. Each individual pixel contains an optical sensor to receive light, a reset input and an electrical output representing the illumination received thereon. The pixel we use here is not a classic pixel since it enables individual pixel reset via an additional transistor [12]. The outputs of a selected row are read through the regular output chain at the lower part, and in addition, are compared with an appropriate threshold, at certain time points in the upper part. If a pixel value exceeds the threshold, a reset is given at that time point to that pixel. The binary information concerning having the reset applied or not is saved in a digital storage, to enable proper scaling of the value read. This enables the pixel value to be described as a floating-point representation. In this representation, the exponent will describe the scaling factor for the actual integration time, while the mantissa will be the regular A/D output. This way, the actual pixel value would be:

$$\text{VALUE} = \text{MAN} * (T/(T/X^{\text{EXP}})) = \text{MAN} * X^{\text{EXP}}$$

where VALUE is the actual pixel value, MAN (Mantissa) is the analog or digitized output value that has been read out at the time point T , X is a chosen constant ($X > 1$), for example, 2, EXP is the exponent value, describing the scaling factor, i.e., which part of the integration time is actually effective. This digital value is read out at the upper part of the chip. For each pixel, only the last readouts for a certain number of rows are kept, to enable the right output of the exponent bits.

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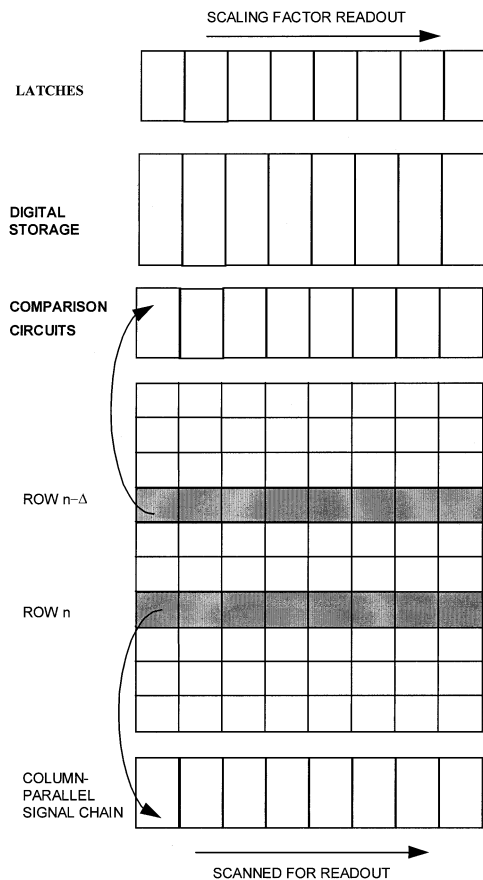


Fig. 1. In-pixel autoexposure CMOS APS—general architecture description.

The idea of having a floating-point presentation per pixel via real-time feedback from the pixel has been proposed before [11]. However, it required an amount of area in the pixel in a way, which substantially affected the fill factor, and it was proposed that the control would be designed as shared for an area of pixels. In the currently proposed solution, the additional hardware required will be placed in the periphery, and the information could be output with minimal effect on spatial or temporal resolution. The spatial resolution would be slightly modified since the desired ability to independently reset each pixel requires an additional transistor per pixel as described in [12]. Concerning the temporal resolution—for a certain pixel we should check at different time points to get the exponential (scaling) term. Equivalently, we could look at the pixels of different rows to get the same information. We could look at row n at time = 0 to get the mantissa (i.e., either through an on-chip or through an off-chip A/D output, the later done at this stage) for row n , while we could look at the pixels in row $n - N/2$ (where N is the total number of rows that set the frame time) to get the first exponent bit ($W1$), as a result of the logic circuit decision for that row. We could also look at row $n - N/4$ to get the second bit ($W2$) for that row, at $n - N/8$ to get the third bit, etc. Thus, at the cost of a customized number of comparisons, we could automatically get the required information, and scale the mantissa accordingly.

Fig. 2 describes the proposed approach via a combined time-space diagram, where the axes represent the row and time, re-

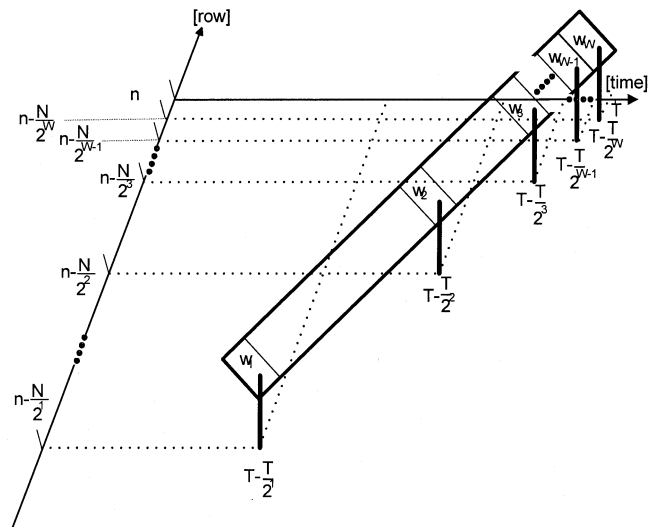


Fig. 2. Combined time-space diagram.

spectively. $W1$, $W2$, etc., represent the exponent bits, i.e., $W1$ represents the point of decision, $T - T/2$, whether to reset or not for the first time, $W2$ for the next point and so forth. The equivalent is shown at point $n - N/2$ in the spatial domain, i.e., that row should be used for the decision concerning $W1$, the first point as described earlier in the time domain.

III. DESIGN AND IMPLEMENTATION

A block diagram of the proposed design is shown in Fig. 3.

In order to share the processing circuits among the pixels in a column, the design makes use of a column parallel architecture. In this architecture, the pixel array, the memory array, and the processing elements are separated.

Each pixel contains an additional transistor, in series with the row reset transistor, activated by a vertical column reset signal that allows the possibility of independent reset of the pixel. With this, the adjustability of integration time can be performed for each pixel, and nondestructive readout of the pixel can be performed at any time during the integration period, by activating the row select transistor and reading the voltage on the column bus.

The processing element contains the saturation detection and the decision logic circuit; it is shared by all pixels in a column. Because of this column parallel architecture, the pixel array contains a minimum amount of additional circuitry and there is little sacrifice in fill factor.

The memory array contains the SRAMs and latches.

Two horizontal decoders for the pixel array and the memory array work in parallel and are used to retrieve the mantissa and exponent, correspondingly. The vertical decoder is used to select the rows in order.

An electrical scheme of each column for implementing the architecture is described in Fig. 4.

The operation of this circuit is described herein. The pixel output signal is evaluated at the comparator, where it is compared with an appropriate threshold.

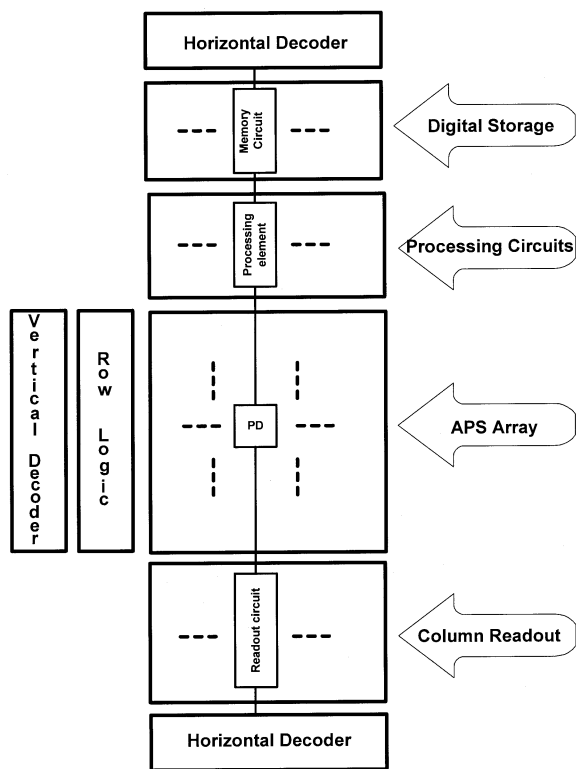


Fig. 3. Block diagram of the proposed design.

The pixel is detected as saturated, if its value does not exceed a pre-determined threshold. Using this information and the binary information concerning the pixel, stored at the memory, at the different parts of the integration, a decision whether to reset the pixel is taken. If the decision is positive, the column reset (CRST) and row reset (RRST) lines must both be precharged at a logical high voltage to activate the reset transistor, and the photodiode restarts integration. When the decision is negative, the reset is not active and the pixel continues to integrate. The binary information whether the reset was applied or not is saved in the SRAM memory storage and output to the latches in due time. Once the row is read through the regular output chain, we retrieve this additional information from the memory through the latches. Comparator mismatch and offset will affect the calculation of the exponent term of the final value. There are different ways to eliminate these problems. In this brief, we aimed to describe the proof of the proposed concept and have not concentrated on comparator offset and mismatch problem details. However, since the comparator resides in the periphery, we can use later an optimum comparator in terms of offset cancellation and mismatch.

IV. EXPERIMENTAL RESULTS

A 64×64 chip was successfully fabricated using regular HP $0.5\text{-}\mu\text{m}$ n-well process available through MOSIS.

The sensor was quantitatively tested for relative responsivity, conversion gain, saturation level, noise, dynamic range, dark current, and fixed pattern noise (FPN). The results are presented below in Table I.

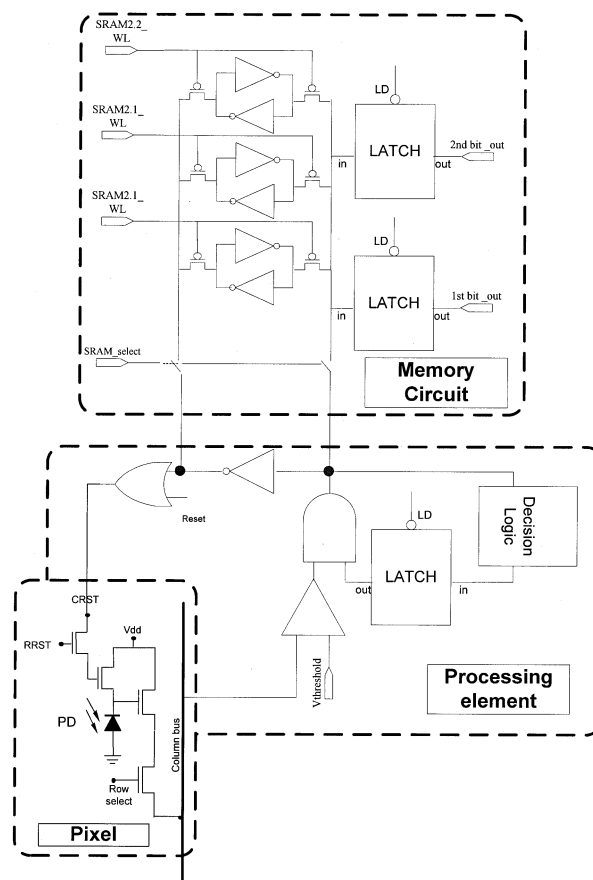


Fig. 4. One column—electrical description.

TABLE I
CHIP ATTRIBUTES

Chip format:	64 x 64
Chip Technology:	HP 0.5um
Chip size:	1.878 mm x 2.9073mm
Pixel size	14.4um x 14.4um
Pixel Type	Photodiode
Pixel fill factor (%)	37%
Conversion gain	12 uV/e ⁻
FPN	0.15%
Dark Current (room temp)	35 mV/sec (0.61 nA/cm ²)
Power	3.71mW (5Mhz)
Inherent Dynamic Range	71.4dB (~11bit)
Extended Dynamic Range	2 additional bits
Saturation level	1.33V
QE	20%

The conversion gain was in general agreement with the design estimate of photodiode capacitance. The saturation level was approximately 1.33 V. FPN was measured to be approximately 0.15% saturation. Dark current were measured to be of the order of 30–35 mV/s, output referred, i.e., 0.61 nA/cm^2 . The inherent dynamic range was 71.4 dB, i.e., 11 bit. The extended dynamic

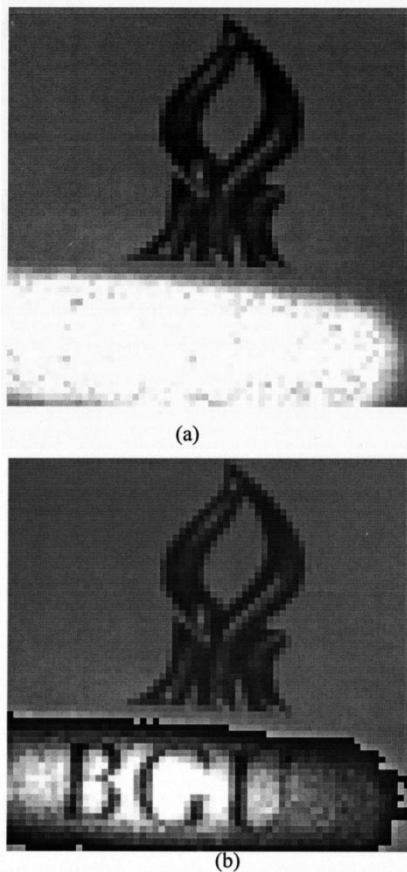


Fig. 5. (a) Scene observed with a traditional CMOS APS sensor. (b) Scene observed with our in-pixel autoexposure CMOS APS sensor.

range consists of two additional bits to this inherent dynamic range. No smear or blooming were observed due to the lateral overflow drain inherent in the APS design.

The chip was also functionally tested.

In the first picture in Fig. 5, a scene is observed, where a strong light (here a laser beam) is pointing to the object and hence part of the pixels are saturated. On the bottom of the picture, you may observe the sensor capability of viewing the details of the illuminated area in real time. Since the display device is limited to eight bits, only the most relevant 8-bit part from each pixel is displayed here, i.e., the mantissa. The exponent value, which is different for different areas, is not displayed.

This concept in its present form suits rolling shutter sensors. It will have problems when motion exists, if speed is higher than frame change. Color reconstruction might also be problematic if individual pixel reset is used. The color version might require limitation of different exposure times per block. In this brief, we demonstrate the concept.

V. CONCLUSION

A proof of concept for a real-time wide intrascene dynamic range APS with customized linear output, which utilizes pixel based control of integration time, adaptive to light, is described. This APS implements a simple function for saturation detection, and is able to control the integration time on a pixel-by-pixel basis, resulting in no saturation. The circuit design of the prototype column based parallel architecture was presented and experimental results obtained with the prototype were described. This in-pixel autoexposure CMOS APS approach releases the limit usually set by the sensor for capturing images with wide intrascene dynamic range.

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