CMOS APS PHOTORESPONSE AND CROSSTALK OPTIMIZATION ANALYSIS FOR SCALABLE CMOS TECHNOLOGIES

Igor Shcherback[1], Orly Yadid-Pecht[1,2], Senior Member, IEEE

1. The VLSI Systems Center, Ben-Gurion University, Beer-Sheva, Israel; shcherba@ee.bgu.ac.il
2. Dept of Electrical and Computer Engineering, University of Calgary, Alberta, Canada; oyp@ee.bgu.ac.il

ABSTRACT

This work presents an improved semi-analytical model developed for photoresponse estimation of a photodiode based CMOS Active Pixel Sensor (APS). We show its use for maximum pixel photosignal prediction and CMOS APS crosstalk (CTK) optimization. Our model reveals the photosignal and the CTK dependence on the pixel geometrical shape and the pixels arrangement within the array. It brings out clearly the possibility of a design enabling maximum response and/or minimum CTK. It can be used, therefore, as a predictive tool for design optimization.

Keywords: CMOS APS, photoresponse and crosstalk.

CMOS APS PHOTORESPONSE AND CROSSTALK MODELING.

It was recently shown [1] that for any pixel active area shape, a reliable estimate of the degradation of image performance is possible, so that the tradeoff between conflicting factors, such as integration photocarriers and conversion gain, could be compared per each pixel design for optimum overall sensor performance. In this work we extend the presented analysis, introduce an improved substrate diffusion effect representation and consider the technology-scaling effect on the device photosensitivity.

$$\frac{V_{out}(\lambda)}{N_{p\lambda}} = \frac{k_1 A + k_2 \left((A + Pd)\left(\frac{S-A}{S}\right)\left(1 - \frac{4Pi - P}{8L_{diff}}\right)\right)}{k_3 A + k_4 P} \quad (1)$$

In this equation k_1 (in μm^{-2}) describes the number of electrons collected by the unity photodiode area in a time unit; k_2 (in μm^{-2}) is the number of electrons collected by the unity "side-wall collecting surface" within the substrate depth, k_3 and k_4 (in aF/μm^2 and aF/μm^1, respectively) describe the bottom and sidewall capacitances. P_i (in μm) is the pixel pitch. P (in μm) is the photodiode perimeter. A (in μm^2) is the photodiode area. $(S-A)$ (in μm^2) is the unoccupied photodiode surroundings area within the pixel. L_{diff} (in μm) is the diffusion length. $V_{out}(\lambda)$ (in V) is the pixel signal output for a particular wavelength, and N_{ph} (in photons/second) is the photon irradiance.

Figure 1 shows the comparison between measured and modeled output curves for the pixel set (square active area shape and decreasing photodiode dimensions fabricated in standard CMOS 0.5μm process) and several wavelengths lighting. The curves share the same behavior and display a pronounced maximum response location.

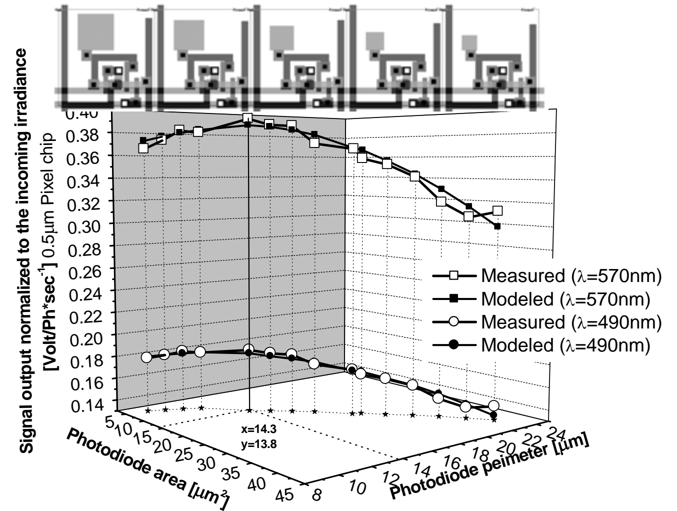

Figure 1: A comparison of the modeled and the measured results obtained for the square active-area pixels (CMOS 0.5μm; the photodiode areas decrease between $40\mu m^2$-$5.5\mu m^2$, and their perimeter varies between $23\mu m$ –$9.3\mu m$) for two different wavelengths. The geometry of the pixel enabling maximum photoresponse is indicated.

Our photoresponse model (Eq.1) enables the extraction of the unity "main area" and unity peripheral contributions to the output signal for the curves in Figure 1 at each wavelength. For a certain process, the combination of the above contributions remains invariable for all pixels (i.e., they are independent of the photodiode shape and size) at a certain wavelength exposure. This enables the prediction and the revelation of the maximum response pixel for any (different!) photodiode geometry without its realization (in a test chip etc.) based on the specific process and design

parameters knowledge only. Moreover, we consider the overall scaling influence on the device sensitivity and propose a first approximation describing the scaling influence and assume that the ratio between the unity "main area" and the unity "periphery" contributions has a slight upward trend, mostly through the reduction of mobility and lifetime with increasing doping levels, and shrinkage of the depletion widths. Thereby with technology downscale, the unity "periphery" contribution to the output signal decreases. Based on the above assumption and using the process data and the results extracted from the 0.5µm chip it is possible to determine the coefficients k_1 and k_2 for the more advanced scalable CMOS 0.35 technology. Considering d as the depletion depth, we predict that:

$$\left.\frac{k_1}{k_2}\right|_{CMOS\ 0.35\mu m}^{570nm} \approx \left.\frac{k_1}{k_2}\right|_{CMOS\ 0.5\mu m}^{570nm} \cdot \left(\frac{d_{CMOS\ 0.5\mu m}}{d_{CMOS\ 0.35\mu m}}\right) \times \left(\frac{L_{n_{CMOS\ 0.35\mu m}}}{L_{n_{CMOS\ 0.5\mu m}}}\right) \approx 1.12$$

$$\left.\frac{k_1}{k_2}\right|_{CMOS\ 0.35\mu m}^{490nm} \approx \left.\frac{k_1}{k_2}\right|_{CMOS\ 0.5\mu m}^{490nm} \cdot \left(\frac{d_{CMOS\ 0.5\mu m}}{d_{CMOS\ 0.35\mu m}}\right) \times \left(\frac{L_{n_{CMOS\ 0.35\mu m}}}{L_{n_{CMOS\ 0.5\mu m}}}\right) \approx 1.07$$

We have examined the total "main area" and the total periphery contributions to the output signal separately as a function of the photodiode dimensions change. With the dimensions decrease, the "main area" contribution scales down, while the periphery contribution scales up, such that their interception indicates the point where the maximum output signal is expected (see Figure 3).

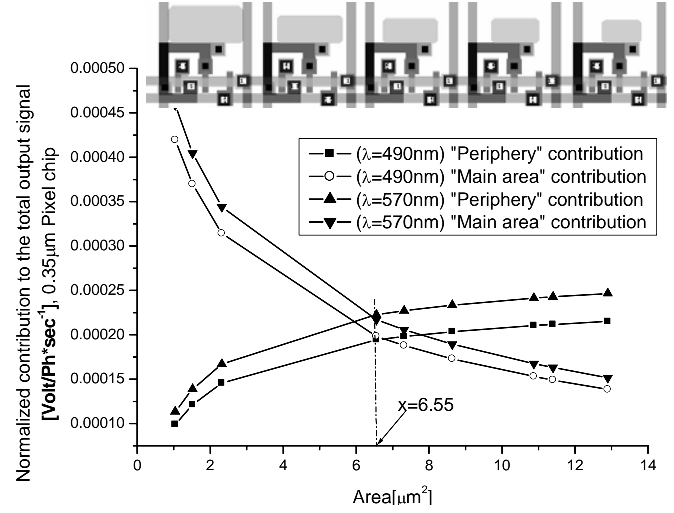

Figure 2: Total "main area" and "periphery" contributions to the output signal as a function of the photodiode dimensions change (CMOS 0.35µm technology, 7µm pixel pitch; the photodiode areas decrease between 13.4μm^2-4.3μm^2, and their perimeter varies between 15μm-8.1μm) for two different wavelengths. Note that this result is obtained theoretically, based on the results analysis obtained from an older 0.5µm CMOS process and scaling considerations only.

Figure 3 shows the comparison between the corresponding measured and theoretically modeled output curves for several wavelengths lighting where an obvious maximum response geometry is indicated. Note that the modeled function reaches its maximum exactly at the point marked by the measurements; moreover, the values obtained by the measurements for the contributions ratio; $k1/k2^{570nm} \approx 1.13$, and $k1/k2^{490nm} \approx 1.068$ are similar to our theoretical results, and the maximum occurs exactly at the predicted interception point. We ratify therefore that our model theoretically predicts the optimal pixel existence and location for scalable CMOS processes, i.e., its geometrical dimensions, based on the process and the specific design data.

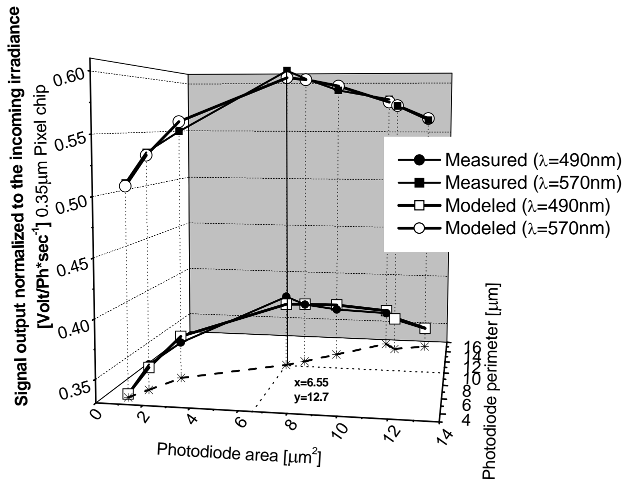

Figure 3: A comparison of the modeled and the measured results obtained for the rectangular active-area pixels. The geometry of the pixel enabling maximum photoresponse is indicated. The maximum occurs exactly at the interception point indicated in Figure 2, i.e., the theoretically predicted result was confirmed by the measurements.

Our unique submicron scanning system (S-cube) [2] use enables a detailed, point by point, quantitative determination of the contributions to the total output signal from each particular region of the pixel (see Figure 4 (A) and (B)).

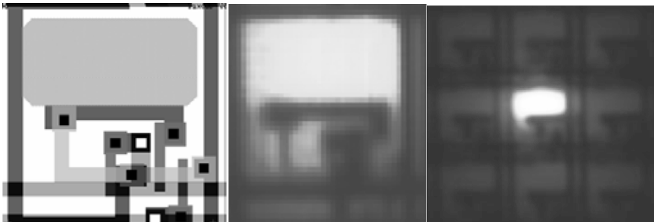

Figure 4: Comparison between pixel design layout (A) and the actual electrical scan result (B). C represents the CTK response map obtained by S-cube system scanning In (B) and (C) the lightest areas indicate the strongest response.

Our photoresponse model, in conjugation with our S-cube system use enables CMOS APS crosstalk magnitude determination and tracking of its main causes. It can be further used as a predictive tool for design optimization. Figure4(C) shows the responsivity map obtained by thorough pixel array scanning [2] (data acquisition was taken at one particular central pixel within a scanned area at each point of the scan). It includes the pixel response and the crosstalk influence and shows that there is an essential difference in the overall CTK obtained from each of the neighbors.

Our photoresponse model enables an accurate estimate of the CTK signals obtained from each neighboring pixel subject to the photodiode shape, size and arrangement within the array. Indeed, the second summand in the numerator of Eq.1 represents the diffusion contribution to the total output signal; thereby it describes also the CTK component (considering the proper geometry, design and process parameters, of course). Hence, in view of the fact that the readout pixel is not illuminated while CTK is measured from its neighbor, the CTK signal can be simply represented as the ratio of the diffusion signal obtained from the neighbor pixel to the overall signal (Eq.1) from the central pixel (the numerators ratio, since the conversion factor of the same acquiring pixel in the denominators cancel). The comparison of the modeled and measured (by S-cube system) CTK values gives an excellent agreement, such the difference is found to be less then 3%.We therefore conclude that a reliable prediction of the CTK in the imager is possible; the proposed method based on our photoresponse model and the S-cube use for CTK measurements enables both its magnitude determination and its main causes discovery, thus enabling design optimization per each potential pixel application.

REFERENCES

[1] I. Shcherback, O. Yadid-Pecht," Photoresponse analysis and pixel shape optimization for CMOS Active Pixel Sensors," *IEEE Trans. Electron Devices,* special issue on Solid-State Image Sensors, vol. 50, pp. 12-19, Jan. 2003.

[2] I. Shcherback, B. Belotserkovsky, A. Belenky, O. Yadid-Pecht, "A Unique Sub-micron Scanning System use for CMOS APS crosstalk characterization" ," Proc. SPIE/IS&T Sym. on Electronic Imaging: Science and Technology, Santa Clara, CA, USA, Jan. 2003.