Point by Point Thorough Photoresponse Analysis of CMOS APS by means of our Unique Sub-micron Scanning System

Igor Shcherback, Tatiana Danov, Boris Belotserkovsky, Orly Yadid-Pecht

The VLSI Systems Center
Ben Gurion University
P.O.B. 653 Beer-Sheva 84105, ISRAEL
Tel: 972-8-6461512
Fax: 972-8-6477620
E-Mail: oyp@ee.bgu.ac.il

ABSTRACT

This work shows the progress and demonstrates the measurements performed via a unique submicron scanning system developed at the VLSI systems center in Ben-Gurion University.
The system enables the combination of near-field optical and atomic force microscopy measurements with the standard electronic analysis. The obtained signal, i.e., the electrical outcome at each point as a function of the spot position provides a 2D signal map of the pixel response, representing the full 3D charge distribution in the device.
This work present the results obtained by thorough scanning of several various pixel topologies of CMOS APS chips fabricated in two different CMOS technologies (the standard 0.5μm and 0.35μm CMOS technologies).
We demonstrate that our system use enables a detailed, point by point, quantitative determination of the contributions to the total output signal from each particular region of the pixel. It makes possible to understand the influence of the each component composing the pixel (e.g., logic transistors, metal lines, etc.) which is extremely important for CMOS APS where the pixel structure defines a fill factor of less then 100%.

Keywords*:* CMOS APS, photoresponse and crosstalk.

INTRODUCTION

Past several years of intensive work, have made Active Pixel Sensor (APS) imagers be considered a viable alternative to CCDs in many application fields. However, in the standard CMOS processes of interest here, there is only a limited choice of photodetector devices. In all reported CMOS imagers, photodetectors were realized by using parasitic elements found in the standard CMOS processes [1, 2]. Relatively low sensitivity to incident light (less than that of CCDs of the same pixel size) reduces the imager efficiency, thereby limiting CMOS APS utilization. Investigations have still to be performed for improving and optimizing APS performance in order to meet dedicated application requirements and to provide designers with better control within the existing technology process boundaries. It appears as important to acquire experimental data concerning parameters affecting electro-optics performance, mainly responsivity, crosstalk, resolution and sensitivity to incident light.

It was recently shown [3] that for any potential pixel active area shape in a particular technology process, a reliable estimate of the degradation of image performance is possible, so that the tradeoff between conflicting factors, such as integration photocarriers and conversion gain, could be compared per each pixel design for optimum overall sensor performance.

In this work, based on the thorough photoresponse investigation performed via our unique sub-micron scanning system we extend the presented analysis and introduce an improved substrate diffusion effect representation. We also consider the technology-scaling effect on the device photosensitivity and propose a simple approximation determining the scaling effect on the overall device photoresponse.

Based on thorough study of the experimental data acquired from several pixel chips fabricated in two different processes, i.e., standard 0.5μm and standard 0.35μm CMOS processes, we show the efficacy and the expediency of our photoresponse model for scalable CMOS processes.

CMOS APS PHOTORESPONSE AND CROSSTALK MODELING

A. Photoresponse Modeling

Figs. 1 and 2 show two subsets of pixels of rectangular and square shapes, with decreasing photodiode active area dimensions, fabricated in a standard CMOS 0.5μm process respectively.

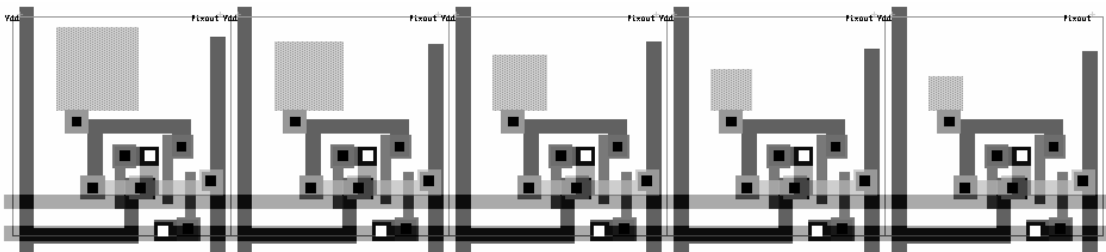

Fig. 1: A subset of square-shaped active area pixels (CMOS 0.5μm technology, 14μm pixel pitch) with decreasing (photodiode) dimensions. The photodiode areas vary between $40\mu m^2$-$5.5\mu m^2$, and their perimeter varies between $23\mu m$ –$9.3\mu m$, after [3].

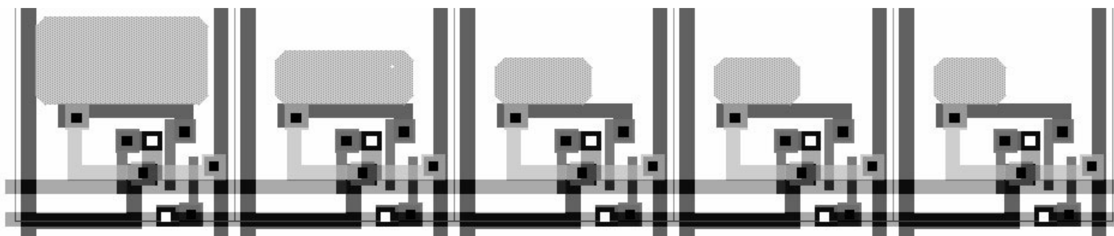

Fig. 2: A subset of rectangular-shaped active area pixels (CMOS 0.5μm technology, 14μm pixel pitch) with decreasing (photodiode) dimensions. The photodiode areas vary between $63\mu m^2$-$13\mu m^2$, and their perimeter varies between $34\mu m$-$15.5\mu m$.

The photoresponse model presented in our " Photoresponse analysis and pixel shape optimization for CMOS Active Pixel Sensors" work[3] enables the extraction (by functional fitting) of the unity "main area" and unity "periphery" contributions to the output signal at each wavelength, and by that the analysis and modeling of the pixels behavior. Fig. 3 shows the comparison between the corresponding measured and modeled output curves for the pixel set presented in Fig. 1 for several wavelengths lighting. It displays a pronounced maximum response location.

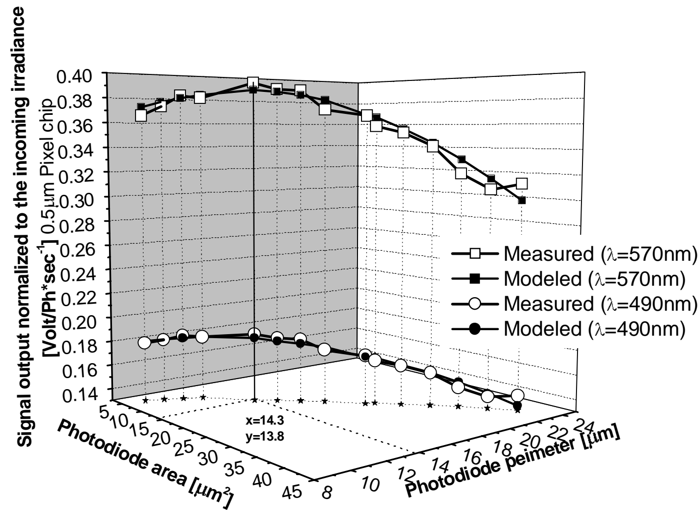

Fig. 3: A comparison of the modeled and the measured results obtained for the square active-area pixels presented in Fig. 1 for two different wavelengths. The geometry of the pixel enabling maximum photoresponse is indicated, after[3].

For a certain process, the combination of the above contributions remains invariable for all pixels (i.e., they are independent of the photodiode shape and size) at a certain wavelength exposure[3]. It enables the prediction and the revelation of the maximum response pixel for any (different!) photodiode geometry without its realization (in a test chip etc.) based on the specific process and design parameters knowledge only. The extrapolation of the modeled function for the rectangular pixels (Fig. 2), envisages the pixel enabling maximum photoresponse (see Fig. 4); hence, the model theoretically predicts its existence and exact geometrical dimensions, which enable the use of that specific design in applications requiring (for some reason, e.g., the additional logic elements in design) the rectangular photodiode shape.

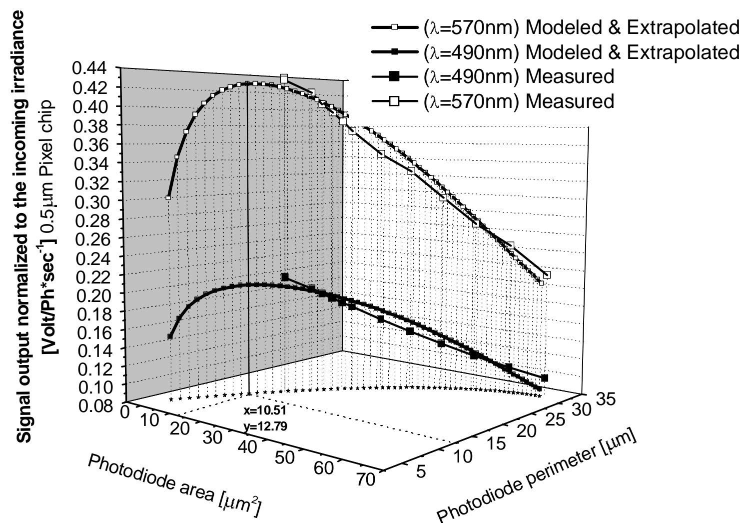

Fig. 4: A comparison of the modeled and the measured results obtained for the rectangular active-area pixels presented in Fig. 2 for two different wavelengths. Model extrapolation envisages the optimal pixel existence and location, i.e., it points out the photodiode area and perimeter corresponding to the pixel enabling maximum photoresponse.

Our unique submicron scanning system (S-cube) [4] use enables a detailed, point by point, quantitative determination of the contributions to the total output signal from each particular region of the pixel (see Fig. 5, 6). The system enables the combination of near-field optical and atomic force microscopy measurements with the standard electronic analysis. The

system obtains an optical signal as input and returns an electrical signal as output. It is capable to hit onto a desirable well-defined point within the scan area. It is able to focus the incoming light signal into the spot of the desirable diameter size (e.g., d<0.5 micron or d<0.35 micron according to the standard VLSI technologies) after penetration through the certain transparent oxide depth without beam broadening, i.e., the desirable size of spot is maintained during the scan.

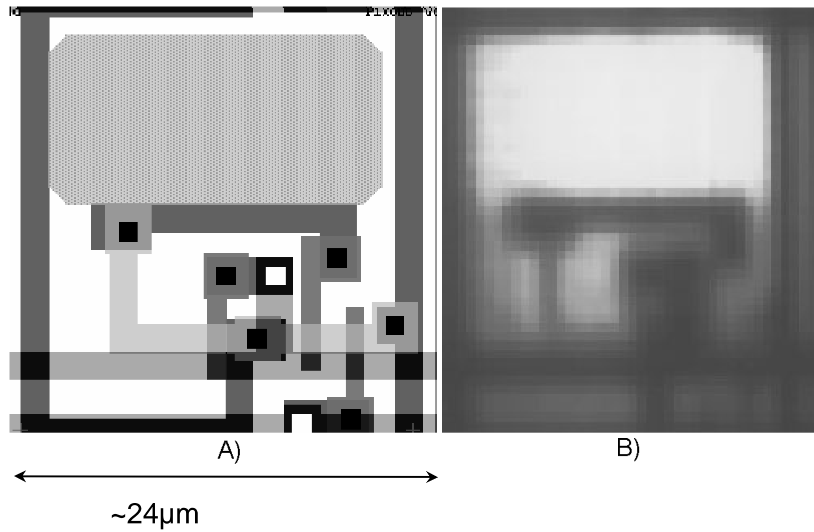

Fig. 5. Comparison between the design layout (A) and the actual electrical scan result (B), obtained by the S-cube system for a pixel fabricated in standard CMOS 0.5µm technology. In (B) the lightest areas indicate the strongest response.

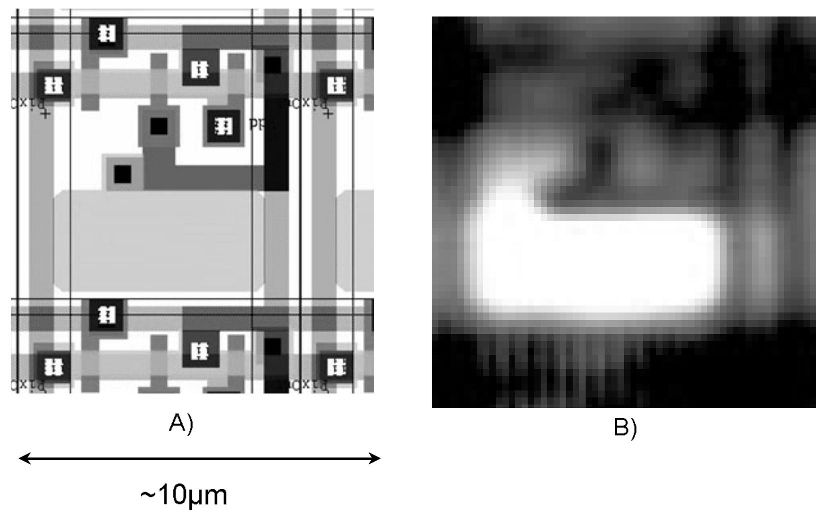

Fig. 6. Comparison between the design layout (A) and the actual electrical scan result (B), obtained by the S-cube system for a pixel fabricated in standard CMOS 0.35µm technology. In (B) the lightest areas indicate the strongest response.

Figs. 5 and 6 show that our system enables an accurate estimate of the contributions to the total output signal obtained from the photodiode itself and from its surroundings, i.e., it is possible to measure the photodiode and its surroundings signal separately.

We have examined the total "main area" and the total periphery contributions to the output signal separately as a function of the photodiode dimensions change. With the dimensions decrease the "main area" contribution scales down, while the periphery contribution scales up, such that their interception occurs exactly at the point where the maximum output signal is predicted by extrapolation (Fig. 4), for the particular CMOS 0.5μm process, see Fig. 7.

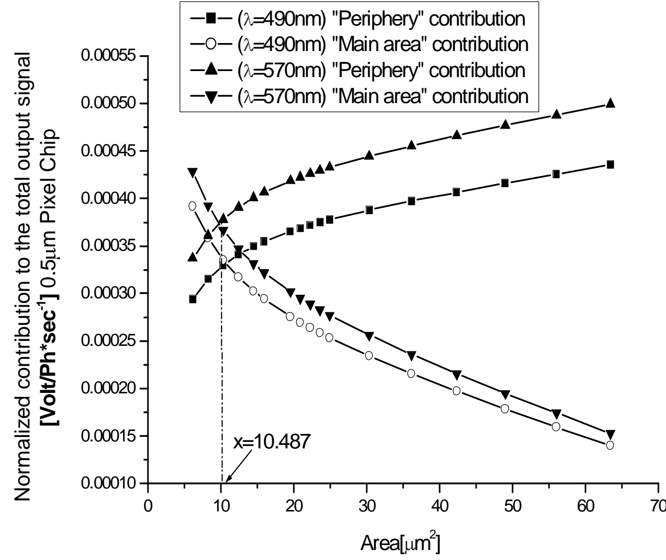

Fig. 7: Total "main area" and "periphery" contributions to the output signal as a function of the photodiode dimensions change for the pixel set presented in Fig. 2. The interception occurs exactly at the point where the maximum output signal was predicted by extrapolation in Fig.4, thus confirming that result.

The overall scaling influence on the device sensitivity is very complicated and depends on a large variety of effecting parameters. An analytical expression, uniquely determining the general scaling trends is not yet developed [5, 6]. We assume that the ratio between the unity "main area" and the unity "periphery" contributions has a slight upward trend, mostly through the reduction of mobility and lifetime with increasing doping levels, and shrinkage of the depletion widths. Indeed, under strong absorption conditions where the diffusion coefficient $\alpha(\lambda)$ and the diffusion length Ln both are much smaller than the substrate width, the photocurrent density through diffusion in the substrate can be derived [6] as $J_{ph} = q\Phi / [1 + 1/\alpha(\lambda) \cdot L_n]$, where Φ is the photon flux entering the quasi-neutral p-substrate region and q – the electron charge. Thereby with technology downscale, the unity "periphery" contribution to the output signal decreases. The depletion width shrinkage means that carriers are collected more through the bottom facet of the depletion region rather than through its lateral facets, intensifying therefore the relative "main area" contribution. Note, in addition, that for advanced processes the junction depth is small in comparison to the absorption depth, such that more photocarriers are collected through the bottom depletion facet.

Based on the above considerations we introduce an improved semi-analytical model developed for photoresponse estimation of a photodiode based CMOS APS. Considering the additional diffusion carriers that can be collected through the bottom depletion facet, the periphery contribution part in our improved model contains an additional $(A + Pd)$ term, describing the wider effective collecting cross section for the lateral diffusion.

$$\frac{V_{out}(\lambda)}{N_{p\lambda}} = \frac{k_1 A + k_2\left((A+Pd)\left(\frac{S-A}{S}\right)\left(1-\frac{4Pi-P}{8L_{diff}}\right)\right)}{k_3 A + k_4 P} \quad (1)$$

Where k_1 (in μm^{-2}) describes the number of electrons collected by the unity photodiode area in a time unit; k_2 (in μm^{-2}) is the number of electrons collected by the unity "side-wall collecting surface" within the substrate depth, k_3 and k_4 (in $aF/\mu m^2$ and $aF/\mu m^1$, respectively) describe the bottom and sidewall capacitances. P_i (in µm) is the pixel pitch. P (in µm) is the photodiode perimeter. A (in μm^2) is the photodiode area. *(S-A)* (in μm^2) is the unoccupied photodiode surroundings area within the pixel. L_{diff} (in µm) is the diffusion length. $V_{out}(\lambda)$ (in V) is the pixel signal output for a particular wavelength, and N_{ph} (in photons/second) is the photon irradiance.

Based on the above assumption and using the process data and the extracted results (the coefficients k_1 and k_2, determining the unity "main area" and the unity "periphery" contributions for each particular wavelength), we propose a first approximation describing the scaling influence, and predict that the coefficients k_1 and k_2 for the more advanced scalable CMOS 0.35 technology can be determined as

$$\begin{aligned} k_1/k_2\Big|_{CMOS\ 0.35\mu m}^{570nm} &\approx k_1/k_2\Big|_{CMOS\ 0.5\mu m}^{570nm}\cdot\left(d_{CMOS\ 0.5\mu m}/d_{CMOS\ 0.35\mu m}\right)\cdot\left(L_{n_{CMOS\ 0.35\mu m}}/L_{n_{CMOS\ 0.5\mu m}}\right)\approx 1.12 \\ k_1/k_2\Big|_{CMOS\ 0.35\mu m}^{490nm} &\approx k_1/k_2\Big|_{CMOS\ 0.5\mu m}^{490nm}\cdot\left(d_{CMOS\ 0.5\mu m}/d_{CMOS\ 0.35\mu m}\right)\cdot\left(L_{n_{CMOS\ 0.35\mu m}}/L_{n_{CMOS\ 0.5\mu m}}\right)\approx 1.07 \end{aligned} \quad (2)$$

where d is the depletion depth.

Substitution of these coefficients into Eq.1 (and using the proper process and design data) while performing a functional photoresponse analysis as the function of the photodiode geometry change enables the theoretical determination of the pixel dimensions enabling its maximum photoresponse.

Consider a set of pixels of a rectangular photodiode shape designed according to the CMOS 0.35µm design rules and obeying the same mathematical guidelines as the pixels presented in Fig. 2. An example subset of these pixels is shown in Fig. 8. Note that all the pixels share a common, traditional three-transistor type readout circuitry, enabling behavior identification of different pixel types, transistor's W/L was scaled 1.5 times from CMOS 0.5µm to CMOS 0.35 µm.

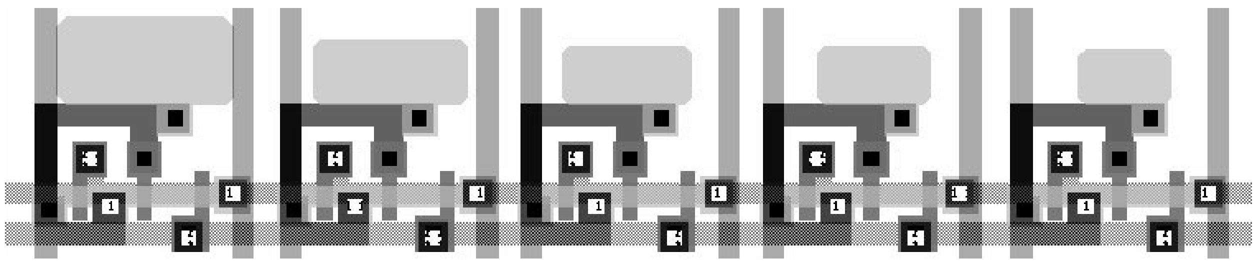

Fig. 8: A subset of rectangular-shaped active area pixels with decreasing photodiode dimensions (CMOS 0.35µm technology, 7µm pixel pitch). The photodiode areas vary between $13.4\mu m^2$-$4.3\mu m^2$, and their perimeter varies between $15\mu m$-$8.1\mu m$.

Fig. 9 shows the comparison between the corresponding measured and theoretically modeled (based on handy processes and designs data) output curves for several wavelengths lighting where an obvious maximum response geometry is

indicated. Note that the modeled function reaches its maximum exactly at the point marked by the measurements; moreover, the values obtained by the measurements for the contributions ratio; $k_1/k_2\big|_{CMOS\ 0.35\mu m}^{570nm} \approx 1.13$, and $k_1/k_2\big|_{CMOS\ 0.35\mu m}^{490nm} \approx 1.068$ are similar to our theoretical results.

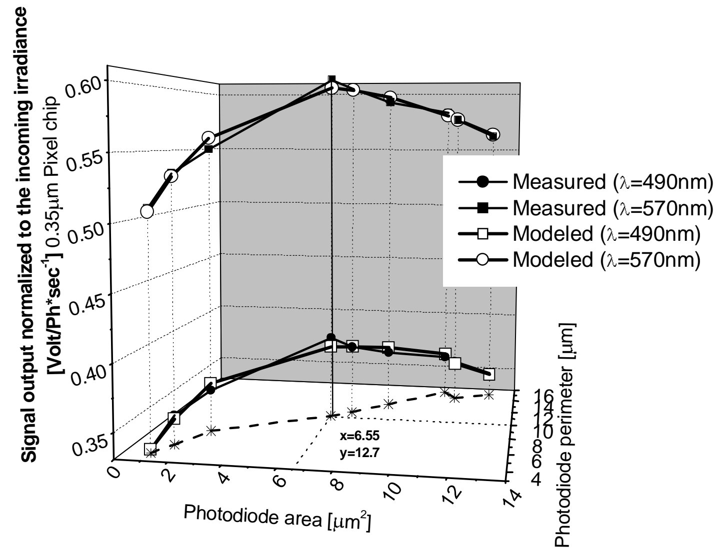

Fig. 9: A comparison of the modeled and the measured results obtained for the pixels presented in Fig. 8for two different wavelengths. The geometry of the pixel enabling maximum photoresponse is indicated.

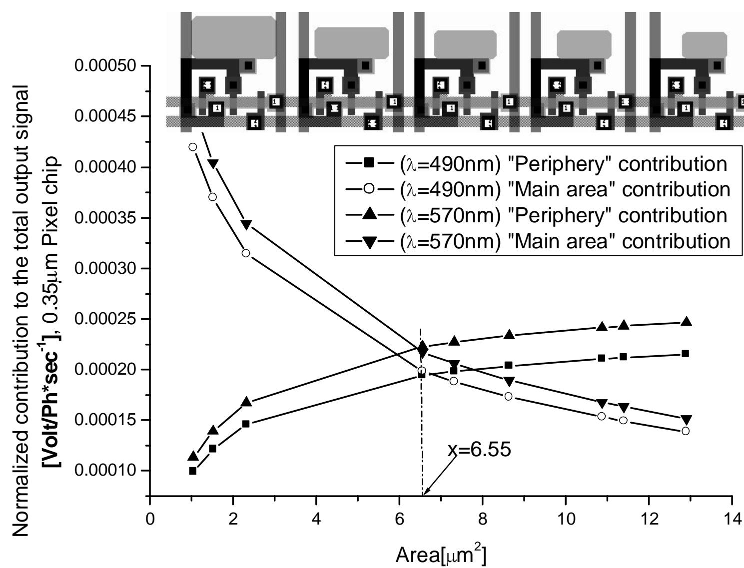

Fig. 10: Total "main area" and periphery contributions to the output signal as a function of the photodiode dimensions change. The interception occurs exactly at the point where the maximum output signal was predicted by the functional analysis, thus confirming that result.

The separate investigation of the "main area" and the periphery contributions to the output signal (see Fig. 10) enables the revelation of the photodiode geometry with the maximum output signal and thus the verification of the presented result. We ratify therefore that our model theoretically predicts the optimal pixel existence and location. i.e., its geometrical dimensions based on the process and the specific design data.

B. Crosstalk Modeling

Our S-cube system use in conjugation with our photoresponse model enables CMOS APS crosstalk magnitude determination and tracking of its main causes. It can be further used as a predictive tool for design optimization.

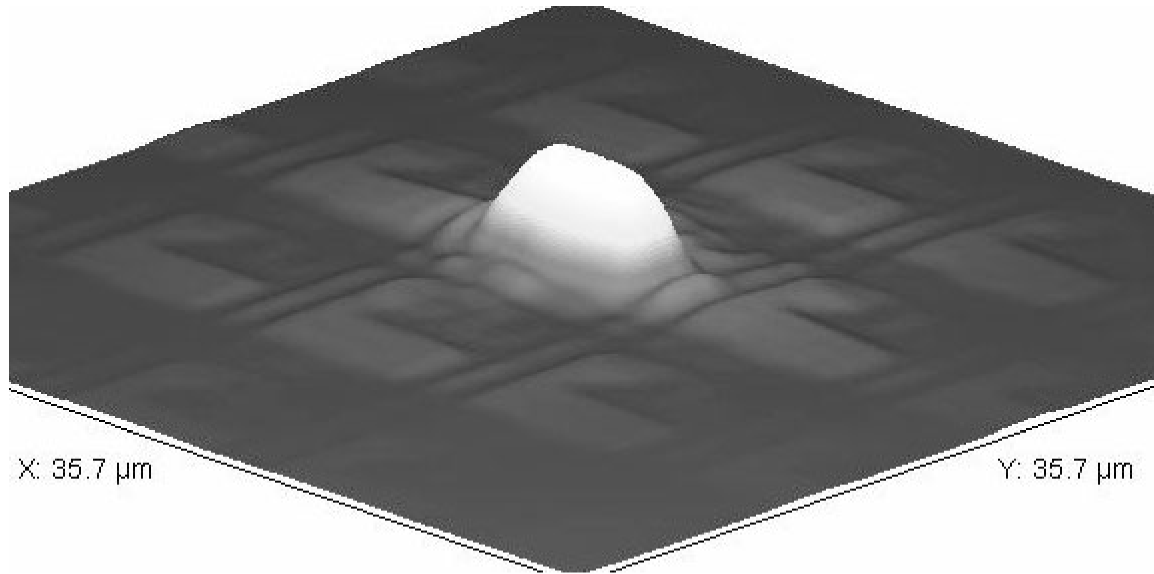

Fig. 11. The 3-D representation of the responsivity CTK map obtained by S-cube system for the array of the rectangular pixels, corresponding to Fig. 6. The lightest areas indicate the strongest response.

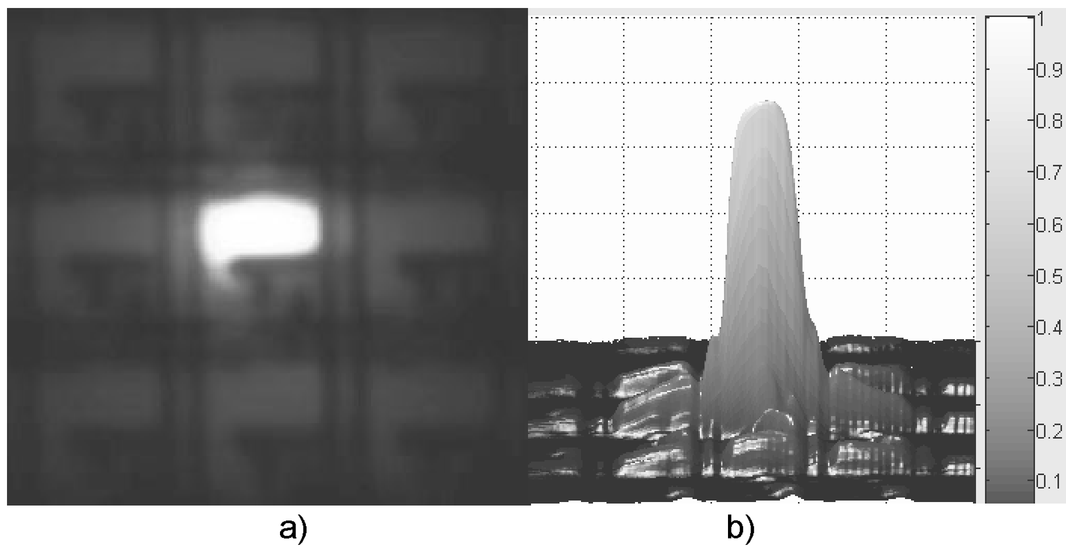

Fig. 12. a) The CTK response map obtained by S-cube system scanning; flat 2-D representation, corresponding to Fig. 11. b) The normalized response; 3-D representation. The lightest areas indicate the strongest response

Figs. 11 and 12 show the responsivity map obtained by thorough sub-micron scanning [4] (data acquisition was taken at one particular central pixel within a scanned area at each point of the scan). It includes the pixel response and the crosstalk influence and shows that there is an essential difference in the overall CTK obtained from each of the neighbors.
Our photoresponse model enables an accurate estimate of the CTK signals obtained from each neighboring pixel subject to photodiode shape, size and arrangement within the array. Indeed, the second summand in the numerator of Eq.1 $k_2\left((A+Pd)\left(\frac{S-A}{S}\right)\left(1-\frac{4Pi-P}{8L_{diff}}\right)\right)$ represents the diffusion contribution to the total output signal; thereby it describes also the CTK component (considering the proper geometry, design and process parameters, of course). Hence, in view of the fact that the readout pixel is not illuminated while CTK is measured from its neighbor, the CTK signal can be simply represented as the ratio of the diffusion signal obtained from the adjacent pixel to the overall signal (Eq.1) from the central pixel (the numerators ratio, since the conversion factor of the same acquiring pixel in the denominators cancel).

$$CTK = \frac{\text{signal from the neigbor pixel collected at the central pixel}}{\text{signal at the central pixel}} \propto \frac{k_2\left((A+Pd)_{central}\left(\frac{S-A}{S}\right)_{neighbor}\left(1-\frac{4Pi-P}{8L_{diff}}\right)_{neighbor}\right)}{k_1 A + k_2\left((A+Pd)\left(\frac{S-A}{S}\right)\left(1-\frac{4Pi-P}{8L_{diff}}\right)\right)\Big|_{central\ pixel}} \qquad (3)$$

The comparison of the modeled (calculated using Eq. 3) and measured (by S-cube system) CTK values gives an excellent agreement, such that the difference is found to be less then 3%. We therefore conclude that a reliable prediction of the CTK in the imager is possible; the proposed method based on our photoresponse model and the S-cube use for CTK measurements enables both its magnitude determination and its main causes discovery, thus enabling design optimization per each potential pixel application.

Summary

In this work, we bring out clearly the possibility of a theoretical prediction for a design enabling maximum output signal extraction (for any potential photodiode shape), based on handy process and design data, for different scalable CMOS technologies. We ratify that first approximation determining the technology-scaling effect expands our photoresponse estimation model [3] field of applicability and enables its use as a predictive tool for design optimization per each potential application in scalable CMOS technologies. Note that since this is the first, simplest model giving a quantitative theoretical value for the pixel photoresponse in various CMOS technologies, further model enhancements are expected to follow.

We also conclude that our method for CMOS APS CTK determination based on S-cube system use enables it accurate measurement and modeling, thereby opening up the possibilities for its optimization and compensation.

Acknowledgments

The authors would like to thank the Israeli Ministry of Trade for supporting this project. In addition, we would like to thank Mr. Alex Belenky for his help in the chip design.

REFERENCES

[1] O. Yadid-Pecht, “*CMOS Imagers course notes*,” Ben Gurion University, 2000.
[2] A. Moini, "Vision chips or seeing silicon", Technical Report, Centre for High Performance Integrated Technologies and Systems, The University of Adelaide, March 1997, (www.eleceng.adelaide.edu.au/Groups/GAAS/Bugeye/visionchips/index.html).
[3] I. Shcherback, O. Yadid-Pecht,” Photoresponse analysis and pixel shape optimization for CMOS Active Pixel Sensors,” *IEEE Trans. Electron Devices*, special issue on Solid-State Image Sensors, vol. 50, pp. 12-19, Jan. 2003.
[4] I. Shcherback, B. Belotserkovsky, A. Belenky, O. Yadid-Pecht, “A Unique Sub-micron Scanning System use for CMOS APS crosstalk characterization”, Proc. SPIE/IS&T Sym. on Electronic Imaging: Science and Technology, Santa Clara, CA, USA, Jan. 2003.
[5] H. Wong, “Technology and device scaling considerations for CMOS imagers,” *IEEE Trans. Electron Devices*, vol. 43(12), pp. 2131–2142, Dec.1996.
[6] T. Lule, S. Benthien, H. Keller, F. Mutze, P. Rieve, K. Seibel, M. Sommer, M. Bohm, “Sensitivity of CMOS based imagers and scaling perspectives,” *IEEE Trans. Electron Devices*, vol. 47, ED-11, pp. 2710-2122, Nov. 2000.