AN APS WITH 2-D WTA SELECTION EMPLOYING ADAPTIVE SPATIAL FILTERING, BAD PIXEL ELIMINATION AND FALSE ALARM REDUCTION

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ABSTRACT

An APS (Active Pixel Sensor) with 2D winner-take-all detection is presented. The system employs adaptive spatial filtering of the processed image with bad pixel elimination and false alarm reduction in case of a missing object. The circuit has a unique ability of adaptive spatial filtering that allows removal of the background from the image, one stage before it is transferred to the WTA detection circuit. A test chip of 64*64 has been implemented in 0.5 µm CMOS technology, 3.3V supply and is expected to dissipate 128mW at video rate.

System operation is discussed and simulation results are presented.

1. INTRODUCTION

One of the advantages of Active Pixel Sensor (APS) arrays is the possibility of fabrication in a commonly used CMOS process, and integration of additional image processing procedures within [1]. This integration can assist in many scientific, commercial and consumer applications, for instance, where spatial acquisition and tracking of the brightest object of interest is sought. The winner-take-all (WTA) function has an important role in this kind of systems, where it selects and identifies the highest input, that corresponds to the brightest pixel of the sensor, and inhibits the others. The result is a high digital value assigned to the winner pixel, and a low one to the others.

Many WTA circuit implementations have been proposed in the literature [2-13]. A good review of some of these basic circuits can be found in [2]. A current-mode MOS implementation of the WTA function was first introduced by Lazzaro [3]. Later, this circuit has been modified by Starzyk and Fang [4] by improving resolution and speed performance. In 1995 DeWeerth and Morris have added distributed hysteresis using a resistive network [5]. At the same time, additional works on voltage mode WTA circuits based on Lazzaro’s work were presented [6,7]. In 1995 this circuit has been modified with feedback and inhibition by Wilson[6] and later, in 1999, by Kalim and Wilson [7]. Another work was proposed by Donckers, Dualibe and Verleysen [7].

Most of these circuits can be integrated with APS sensors. Some of them were designed especially for image processing, in which the inputs are not stationary [9]. Most of the works describe a one-dimensional, n-element array of the WTA. A few [10,11], discuss 2D arrays. In [11] the image processing circuitry is included in the pixel with payment in fill factor or pixel size and resolution. As mentioned above, the regular WTA circuit chooses a winner from a group of input signals. So, a number of problems can occur when the APS with WTA selection system is used for object selection. The first one occurs when the object of interest disappears from the processed image. In this case the WTA will compare the input voltages that represent intensity levels of the image background. Hence a necessity for background filtering exists. The second problem that can disrupt proper operation of the system is a bad pixel. It can have a very high value, so it can be selected as the winner regardless of other pixel values.

Several techniques for background filtering have been presented in literature [12,13]. This filtering is based on techniques for replacing values of low image intensity levels with zero (thresholding). In [12] the signal is compared against a globally set threshold, above which pixels qualify as object pixels. The disadvantage of this kind of filtering is that it is necessary to choose the value of this threshold in advance and in the case where the background is sufficiently bright (above the chosen threshold), the circuit will not be able to cope with the task. The worst case is if the object of interest disappears from the processed image and the background is bright.

In [13] another technique for background filtering has been proposed. The filter circuit is connected between the APS outputs and the regular WTA circuit inputs. This filter solved most of the problems mentioned above, but still not adaptive.

The system proposed in this paper is a 64*64 element APS array with two-dimensional WTA selection and spatial adaptive filtering circuits, which allows adaptive background filtering and false alarm reduction in case of a missing object. The proposed system also allows bad pixel elimination.

Section 2 describes the system architecture that was implemented. The detailed circuit description is presented in Section 3. Section 4 describes the system performance including simulation results. Section 5 concludes the paper.

2. SYSTEM ARCHITECTURE

Fig 1. shows the block diagram of the proposed system. There is no penalty in spatial resolution using our architecture, the processing is done at the periphery. The process of phototransduction in APS is performed in two stages: (1) The Reset stage (the charging of a photodiode capacitor to a high reset voltage) (2) The Signal stage (the discharging of the capacitor through a constant integration time. In our proposal the commonly used Correlated Double Sampling (CDS) circuit which subtracts the signal pixel value from the reset one is performed on chip. The CDS output is high for a bright pixel and low for a dark one. The following stage is adaptive background filtering of all pixels of which the CDS values are less than a threshold. This threshold corresponds to the average of outputs from all row sensors, with an addition of a small varying epsilon value. The next stage is the winner-take-all selection done by a simple voltage mode WTA after [8].
The main factor for choosing this WTA circuit is its simplicity. Generally, any kind of voltage/current mode WTA can be integrated with this system [13]. The 1-D winner selection array was designed to consist of 8 identical blocks of 8-input WTA cells to achieve better resolution and reduce matching problems. The row winner value is stored in the analog memory that corresponds to the actual row, its column address is stored in a corresponding digital memory (both analog and digital memories are placed in Row logic block in Fig.1). In case of “no object” in the row, the value that is transmitted to the memory is zero. Following a full frame scan, the WTA function is activated on all 64 row winners (row WTA block in Fig.1), the location of the global frame winner is found and the analog value with the address are readout of the memory.

This kind of architecture allows to enlarge the proposed system to any N*N size array without affecting the system properties.

3. CIRCUIT DESCRIPTION

3.1. An adaptive spatial filter

The principle scheme of the adaptive 1D filter circuit is given in Fig 2. The inputs to the filter correspond to the CDS values and the “control” signals are output. As was mentioned before, the circuit filters all pixels of which the CDS values are less than a threshold. This threshold corresponds to the average of outputs from all row sensors, with an addition of a small varying epsilon value. The “control” value is high in case of an object pixel and low if the pixel is a background one. The advantage of this newly proposed filtering is that this epsilon value is adaptive and not constant for different input vectors. The value of epsilon depends on the average current value - it increases when the current average decreases, and decreases when current increases. This results in a small epsilon value in case of high background and a high epsilon in case of a low one. This way, the filtering process is more sensitive when a high background is present and the object’s input voltage is very close to the background. The epsilon value can be controlled manually by setting suitable V- and V+ voltage values (see Fig. 2).

If the V+ is zero and V- is VDD, then the epsilon value is zero and all \( I_{average} + \epsilon \) currents of the circuit are equal to the average current of the n inputs in an n sized array. The non-zero epsilon value can be added to this average by increasing the V+ value. The epsilon value can also be subtracted from the average by decreasing V+ value. Usually we are interested in a positive epsilon value, so V- is VDD. Note that the voltages to current converters have a pull configuration (the current direction is shown by arrows in Fig. 2).

The adaptive functionality can be achieved by operation of N transistor in the linear region. With average current increase (reflecting background increase), Vgs of the \( P_{1} \ldots P_{N} \) transistors are increased too, which causes reduction of N Vds voltage. The result is a fall in N current and reduction of epsilon. Note that if one wants to achieve a constant epsilon value, a stable current source that does not depend on Vsg of \( P_{1} \ldots P_{N} \) can be used instead of N. Another simple option is to connect two parallel transistors instead of N: the first, with large W/L value operated in saturation and another, with a small W/L operated in the linear region. This way a constant epsilon can be achieved by cutting-off the transistor, which is usually operated in the linear region and using only the saturation transistor, or, instead, have an adaptive epsilon value by a linear region operating transistor and cutting-off the other one.

In addition to this background filtering, the circuit enables “no object” notification. If the control values of all pixels are ‘0’, the “no object” function is positive.
The inputs to the WTA circuit depend on the filter control values – zero in the case of a background pixel, and pixel intensity level in the case of an object one. This way false alarm is reduced.

### 3.2. Bad pixel elimination

One problem that can disrupt proper operation of the system is a bad pixel. It can have a very high value, so it can be selected as the winner regardless of other pixel values. In the proposed system bad pixels are disabled in a special “dark mode”, in which a dark image is input. Fig. 3 shows the principle scheme of the bad pixel elimination mechanism.

The bad pixel elimination is realized in two stages. In the first one, the “dark mode" stage, we process a dark image and the circuit finds “bad" bright pixels and saves their addresses. In this stage the signal “dark_mode" is ‘1’. In the second one a real image is processed and “bad" pixels the found in the “dark mode" stage are replaced by ground values.

When the signal “dark_mode" is ‘1’, the circuit starts to work in “dark mode". The bad pixels are located by the regular WTA operation of the system. After each additional frame scanning a new bad pixel is found and its address is stored in memory. In the regular system operation, when a real image is processed, the “in_addr" value (that corresponds to row address in APS) is compared with the Y_addr stored in the memory. If their values are equal, the comparator will output ‘1’ and the X_addr of the 1’st frame winner (the column address of the first found bad pixel) directed to Dec6*64. The switches array replaces input voltage with ground one according to the decoder’s output (if the output is ‘1’, then voltage is replaced). In this way all bad pixels values are replaced by ground.

The system proposed in this paper allows eliminating up to 3 bad pixels. Adding same logic can easily increase the number of the bad pixels that the system allows to eliminate.

### 4. PERFORMANCES AND SIMULATED RESULTS

The proposed 64* 64 APS array with WTA selection was designed and fabricated in the 0.5um, 3.3V, n-well, 3-metal, CMOS, HP technology process supported by MOSIS.

The circuits were simulated with the SPECTRA Cadence simulator using HP 0.5um CMOS process parameters. The supply voltage is 3.3V. Fig. 5 shows the layout of the chip.

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**Fig. 2. Spatial filter circuit - principal scheme.**

**Fig. 3. The principle scheme of the bad pixel elimination mechanism.**

**Fig. 5 Chip Layout.**
An example of a possible input image in image processing applications for object tracking is shown in Fig 6(a). Fig 6(b) shows the effect of spatial filtering on the image and the global winner location simulated by Matlab.

![Input image example](image1)

![Simulated effect of spatial filtering on the image](image2)

Fig.6. (a) Input image example, (b) Simulated effect of spatial filtering on the image.

Table 1 summarizes the chip specifications.

<table>
<thead>
<tr>
<th>Technology</th>
<th>HP 0.5um</th>
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<tr>
<td>Voltage supply</td>
<td>3.3V</td>
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<tr>
<td>Area size array</td>
<td>64*64</td>
</tr>
<tr>
<td>Pitch width</td>
<td>14.4um</td>
</tr>
<tr>
<td>WTA mode</td>
<td>Voltage</td>
</tr>
<tr>
<td>WTA resolution</td>
<td>40mV</td>
</tr>
<tr>
<td>Chip size</td>
<td>3.5*4.3mm</td>
</tr>
<tr>
<td>Frame scanning frequency</td>
<td>30Hz</td>
</tr>
<tr>
<td>Typical power dissipation (the objects is 12.5% of the frame)</td>
<td>~128mW</td>
</tr>
<tr>
<td>Max allowed power dissipation (the objects is 80% of the frame)</td>
<td>~0.8W</td>
</tr>
</tbody>
</table>

Table 1. Expected chip attributes.

5. CONCLUSIONS

System description, circuit design and simulation of a 64*64 element APS array with two-dimensional WTA selection, bad pixel elimination and spatial adaptive filtering circuits, which allows adaptive background filtering and false alarm reduction have been presented. The system can be easily enlarged to any N*N size array.

A prototype chip is being fabricated in a 0.5 µm HP process. It operates of a single 3.3V supply and is expected to dissipate 128 mW at video rate (when 12.5% of the entire frame are different bright objects and 87.5% is a background). The circuit has a unique ability for adaptive spatial filtering that allows removal of the background from the image and false alarm reduction. The filter uses a “smart” average + ε computation circuit that allows to achieve an adaptive epsilon value that depends on the background level.

In the proposed system bad pixels are disabled in a special “dark mode”, in which a dark image is input. Adding logic can easily increase the number of the bad pixels that the system allows to eliminate.

The circuits were simulated with the SPECTRA Cadence simulator using HP 0.5um CMOS process parameters in order to receive expected chip attributes. The Matlab simulations have been done in order to check effect of spatial filtering on the processed image.

At this stage the chip is in fabrication and we expect to report test results at the conference.

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REFERENCES