

Paper Title:

**6.7 “Autoscaling CMOS APS”**

Authors:

Orly Yadid-Pecht and Alexander Belenky

Affiliation:

Electrical and Computer Engineering Department,

Ben-Gurion University, P.O.B. 653, Beer-Sheva 84105, Israel

e-mail: [oyp@ee.bgu.ac.il](mailto:oyp@ee.bgu.ac.il)

Speaker:

Orly Yadid-Pecht

In recent CMOS and CMD solutions it has already been shown that an ultra high wide dynamic range using two samples per frame could be achieved [1, 2]. However, this will work well if the illumination levels are suited to one of the two integration times. If the illumination ranges somewhere in between, an accurate reading will not result. Multiple outputs could be read for different integration times. Yet, an additional frame memory for each extra reading is required, and also some synchronization process needs to be done since the readings will be set apart in their starting point.

A different architecture, achieving a wide dynamic range via more than two samples was recently suggested [ 3]. It requires, however, a large pixel area and in that proposal the extra circuitry was divided between four neighboring pixels. Another sensor achieving a wide dynamic range was also proposed recently [4]. It requires, though, non-standard CMOS technology and a larger pixel area.

The architecture of our new proposed approach is shown in Fig.6.7.1. Every row is read through the regular output chain, at the lower part, and in addition is compared with an appropriate threshold, at certain time points. If a pixel value exceeds the threshold, a reset is given at that time point to that pixel. The binary information concerning having the reset applied or not is saved in digital storage so that the exact illumination level could be scaled appropriately. This way the pixel value could be described as a floating point representation. In this representation, the exponent will describe the scaling factor for the actual integration time, while the mantissa will be the regular A/D output. This way, the actual pixel value would be:

$$\text{VALUE} = \text{MAN} * (\text{T}/\text{X}^{\text{EXP}}),$$

where VALUE is the pixel value which consists of the MAN (Mantissa, the analog or digitized output value), multiplied by the actual integration time, which is a function of the full integration time, T. The full integration time is divided by a constant X, for example 2, to the power of EXP. EXP is the exponent value, describing the scaling factor, ie which part of

the integration time is actually effective. This value is read out at the upper part of the chip.

The idea of having a floating point presentation per pixel via real time feedback from the pixel has been proposed before [5]. However, it required an amount of area in the pixel in a way which substantially affected the fill factor, and it was proposed that the control would be designed as shared for an area of pixels. In the currently proposed solution, the additional hardware required will be placed in the periphery, and the information could be output with minimal effect on spatial and temporal resolution. The spatial resolution would be slightly modified since the desired ability to independently reset each pixel requires an additional transistor per pixel [6]. Concerning the temporal resolution - for a certain pixel we should check at different time points to get the exponential (scaling) term. Equivalently, we could look at the pixels of different rows to get the same information. We could look at row  $n$  at time=0 to get the mantissa (i.e. the regular A/D output) for row  $n$ , while we could look at the pixels in row  $n-N/2$  (where  $N$  is the total

number of rows that set the frame time) to get the first exponent bit (W1) for that row. We could also look at row  $n-N/4$  to get the second bit (W2) for that row, at  $n-N/8$  to get the third bit, etc. Thus, at the cost of a customized number of comparisons, we could automatically get the required information, and scale the mantissa accordingly.

Fig. 6.7.2 describes the proposed approach via a combined time-space diagram, where the axes represent the row and time, respectively. W1, W2, etc, represent the exponent bits, i.e. W1 represents the point of decision,  $T-T/2$ , whether to reset or not for the first time, W2 for the next point and so forth. The equivalent is shown at point  $n-N/2$  in the spatial domain, i.e. that row should be used for the decision concerning W1, the first point as described above in the time domain.

Fig. 6.7.3 describes the first chip, which was designed using the HP 0.5 $\mu$ m n-well process available through MOSIS. This chip was already tested. In the first picture in Fig. 6.7.4, a scene is observed, where a strong light (here a laser beam) is pointing to the object and hence part of the pixels get saturated. On the

bottom, you may observe the sensor capability of viewing the details of the illuminated area in real time. Since the display device is limited to 8 bits, only the most relevant 8 bit part of the whole 16 bit range from each pixel is displayed. Table 6.7.1 summarizes the chip specifications.

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