

A Random Access Photodiode Array for Intelligent Image Capture

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Abstract - A novel chip implementing random scan was designed, fabricated and tested. The chip covers the basic requirements for random access and separation between the sampling and reading processes. In this way a repeated reading of any pixel at any time can take place. The chip includes an 80×80 matrix of basic cells. Each cell consists of two stages: the first is based on a switch while the second includes a buffer. The chip was fabricated in a 3μ CMOS process. It was found to operate functionally. However, the use of a standard process gave rise to the crosstalk phenomenon which has yet to be overcome.

1. Introduction

Detector array technologies have been developed with the advance of microelectronics and VLSI (Very Large Scale Integration). The solid state imagers which are discussed here use the electro-optical properties of semiconductor materials for sensing electro-magnetic radiation. Signal processing units can be attached to the detectors at the focal plane of the optical system. The output signals are typically read sequentially, using electronic scanning techniques. The two-dimensional array is an expansion of the linear array concept, which by itself is the expansion of the single detector element.

Charge transfer techniques are the most common method used by two-dimensional imaging arrays. In this approach, photo-generated charge is collected and transferred in a pre-determined way.

The two common charge transfer technologies used are charge-coupled devices (CCD) introduced by Boyle et al. [1] and charge injection devices (CID) proposed by Burke and Michon [2]. The advantages and disadvantages of these methods are summarized for example by Barbe [3]. In addition to charge transfer devices, other concepts for discrete optical detector arrays have been implemented. One common concept is an array of light sensitive p-n semiconductor junctions, also called photodiodes.

The main advantage of the photodiode array over the charge-transfer devices is the simplicity of fabrication - it does not require special technology, a conventional MOS process is sufficient. However, in order to obtain better sensors, special "tailored" processes were developed. This will be further discussed in the concluding section. Another advantage of the photodiode array is that random scan can be easily implemented, as each pixel can be accessed separately, unlike in charge transfer devices.

The main goal in this design is the availability of random access. Every pixel can be reached independently by this approach. Although the array acquires all the information, part of it might not be read at all. On the other hand, there might be parts of the information that will be read more than once. This design, with the availability of Random Access concept has its use in intelligent scan systems [4]. It imitates the eye operation in which there is a foveating system that scans the picture by controlling eye ball movement. The result is a non-uniformly scanned picture. The sensor described here allows selective data acquisition.

The design contains an addressable array. Each cell consists of a light detector, information holding and read out circuits. In order to decouple between the light detection and the algorithms of computer vision that decide which pixels to read, and in order to prevent interdependence between them, the processes are separated, i.e., the light sensing is periodical but reading can take place at any time. Furthermore, the algorithm is allowed to read a pixel more than once (before it is sampled again).

Several alternatives for designing the basic cell were considered and the best alternative was chosen for the final design. A chip of

80×80 cells was designed, fabricated and tested. It was found to work functionally. However, the use of a standard process (that is mainly implemented for digital circuits) gave rise to the crosstalk phenomenon. As a conclusion, we have to find resources to overcome this problem.

Section 2 describes the chip overall design concepts, while section 3 deals with the unit cell design concepts. Section 4 describes the basic cell configuration and section 5 describes the chip performance. Section 6 concludes the paper.

2. Chip Design Concepts

The chip architecture is similar to that of random access memories (RAM). The advantage of this architecture is that the location of important video data can be immediately accessed and processed without wasting time on non-relevant video data. The overall design is shown in Fig. 1. A two-dimensional array of R rows and C columns of imaging cells occupies most of the chip area. Readout is accomplished by addressing the row and column of a particular pixel. The row is accessed by a row decoder which selects one of the R output lines. Simultaneously, the columns carry the contents of the R'th row. Each column bus is connected to the single output bus through the column selector which consists of switches (pass transistors) controlled by a column decoder. The output bus is further connected to an output amplifier that transfers the analog information out.

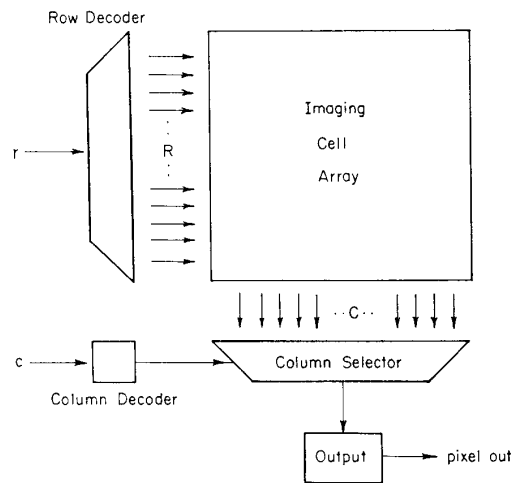


Fig. 1: General chip design.

The two basic design principles in this chip design are:

- Enabling random access to each pixel;
- Separating the sensing section from the readout in such a way that each pixel can be read at any time during the integration period. Multiple readings of the same pixel are possible. This second principle demands a special cell design, which is discussed in the following section.

One of the design goals was to achieve maximum speed in minimum area. However, a scanning circuit for each row and each column is provided, to enable random scan. The integration period was chosen to be uniform for all pixels in order to simplify the individual pixel design and minimize its size. The matrix area fills around 65% of the total chip area.

3. Unit Cell Design Concepts

The basic cell organization is shown in Fig. 2. The input signal to each pixel is the light intensity at that location. It is transduced by the sensor and its associated circuits to an analog voltage at the output. The sensing is done via a reverse biased photodiode, which is reset periodically to a fixed bias. The diode collects the photogenerated electrons and discharges in proportion to the integration period and the diode photocurrent. The cell includes a Sample and Hold circuit (S&H, A1), which forms the first stage, a memory capacitor (C1), and a second stage denoted by (A2). The design realizes the required separation between the sensing and reading processes. The memory capacitor C1 will keep the sampled value for additional readings in the same integration period.

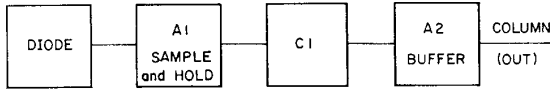


Fig. 2: Basic cell - block diagram.

The pixel size should be minimized in order to achieve higher resolution. Therefore only n-type channel transistors were used in each cell, although the chip was fabricated using CMOS technology. In general, the cell operation consists of three parts: (a) sensing, (b) sampling, and (c) reading.

After the desired integration period the signal is sampled and transferred to the memory capacitor. The voltage on the capacitor depends on the transfer function of the sample unit A1 (see Fig. 2). A1 can be either a voltage follower buffer or a switch which transfers some of the charge stored in the photodiode depletion capacitance into the memory capacitor. In the latter case, the capacitor should be precharged to a starting voltage before the sampling.

This design allows the separation of the reading from the sensing. The reading may occur several times during the sensing of a new value, while the sample and reset switches are off. For reading, the row-select switch closes and the voltage is transferred to the column bus. The voltage depends of the transfer function of A2 (see Fig. 2). Reading will be accomplished by closing the column-select switch to pass the column value to the output.

4. Basic Cell Configuration

Several configurations were considered for the basic cell, differing in the implementation of the A1 and A2 units. The first was a pure Sample and Hold circuit with switches only. Other possibilities included using one or two buffers separating the different parts of the cell. All possibilities are described thoroughly in [5].

The preferred configuration includes one buffer, placed between the capacitor C1 and the output column. This is schematically shown in Fig. 3a. The buffer is implemented as a source follower, in which transistor M5 is its upper part (see Fig. 3b). The current source is shared among all cells of the column. In this design A1 is implied with a pass transistor (M4), so that charge sharing takes place between the diode and the capacitor. M9 is the RSel (Row Select) transistor that is a part of each cell, while the CSel (Column Select) transistor connects the column transistors to the output amplifier. In addition, transistors M1 and M2 are needed for resetting the diode and capacitor correspondingly. Fig. 3c shows the timing diagram for the basic cell.

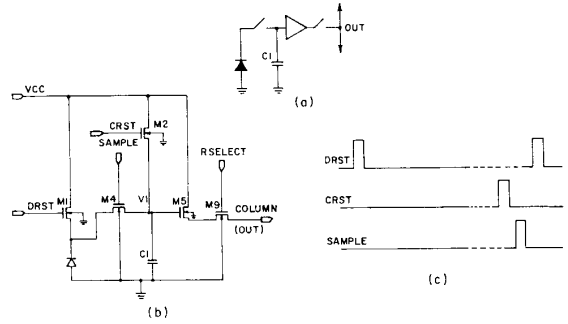


Fig. 3: Basic cell electrical description:

- a. Schematic description;
- b. Electrical description;
- c. Signal timing;

Diode is reset (DRST) at the beginning of the integration interval. At the end, the memory capacitor is reset (CRST), followed by sample. Subsequently, the diode is reset again.

Fig. 4 shows the simulation results for this design, with integration intervals of $3\mu\text{sec}$. At $t = (3n)\mu\text{sec}$, $n = 0, 1, \dots$ the diode and capacitor are precharged. This takes about 50nsec when minimum size transistors of $3\mu\text{m}$ CMOS are employed. At $t = (3n+1)\mu\text{sec}$, sampling is done and the capacitor voltage (V_{C1}) changes in proportion to the diodes voltage (V_d). Sampling takes about 10nsec . Note again that the discharging current was changed in this simulation from one integration interval to another.

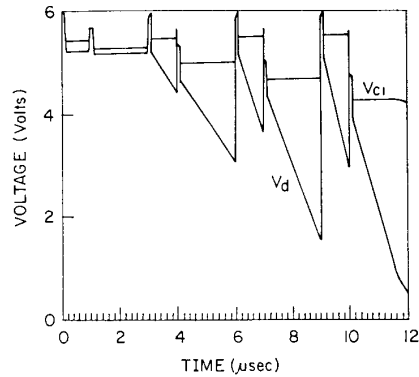


Fig. 4: Simulation of the first stage with a pass transistor: V_d is the simulated diode voltage, V_{C1} is the simulated voltage on capacitor C1.

5. Performance Analysis

A linear approximation for the diode and capacitor voltage in proportion with light is given in [5]. A graph describing this approximation is shown in Fig. 5. Noise analysis was performed with results of about 60dB (see [5]). A chip including an 80×80 matrix in a $7.9\text{mm} \times 9.2\text{mm}$ was fabricated in a $3\mu\text{m}$ CMOS process. Fig. 6 describes the chip layout. In addition, a test chip including smaller matrices and bigger cells was fabricated too. Only experimental results of the fabricated chips will be summarized here.

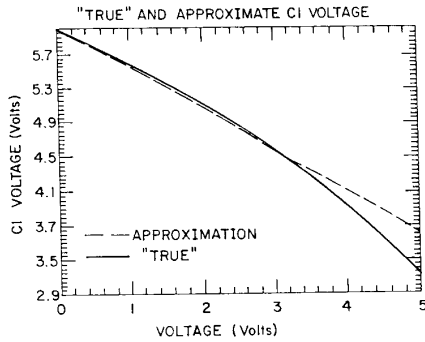


Fig. 5: "True" and approximate capacitor(C1) voltage.

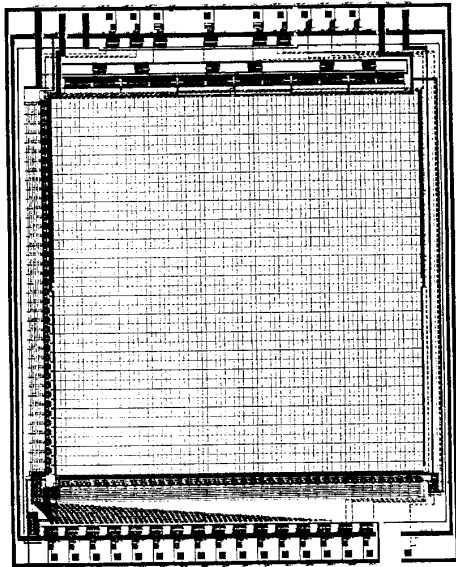


Fig. 6: Overall chip layout.

As described earlier, the diode discharges in proportion to the light intensity and the integration period. During the sampling phase, the diode charge is shared with the capacitor. The "sampled" charge on the capacitor should remain constant till the next sampling.

Fig. 7 shows sampling at different light levels of the diodes from the test chip. Note that the value of the sampled voltage depends on light intensity properly. However, the tests show that the unwanted memory capacitor discharge due to light is much stronger than predicted by the "dark current" leakage process. We would expect the sampled voltage on the capacitor to remain constant. However, it clearly discharges: The stronger the light, the faster the discharge. As the capacitor is actually a combination of several capacitors, in which diffusion capacitance contributes around 30%, this can be due to the carriers generated under the exposed diode having lifetime long enough to diffuse and discharge the capacitor even though it is protected from light.

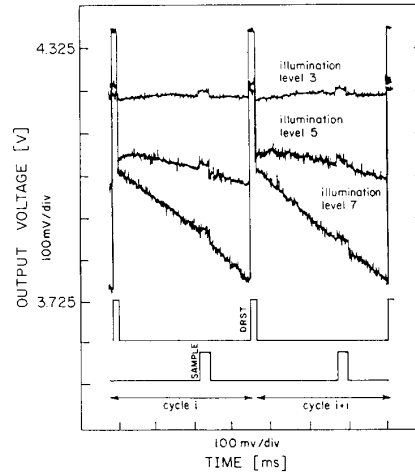


Fig. 7: Sampling different illumination levels.

The effect described above is also referred to as crosstalk which describes photocarriers that affect nodes which are far from the original illumination [6]. The main contribution to the crosstalk here is electrical: the discharge of near cells due to the long lifetime minority carriers. This was further checked as explained in the following.

The minority carriers lifetime dependence on temperature in silicon at the 270K - 350K range is approximately linear [7]. The accurate function is complicated, and attaining a theoretical explanation of the empirical tests depends on the assumption of trap cross-section (σ) and depth side in the forbidden gap that change with temperature.

The chip was cooled using fluid Freon, to about -20° - -40° C (roughly estimated). By comparing the results in the big test cells before and after the cooling, it was found that after cooling a stronger discharge occurred in the illuminated cell, while the discharge in the adjacent cells became negligible (see Fig. 8). On the other hand, at room temperature the adjacent cells are strongly influenced by the illuminated diode. This agrees with the assumption that the lower the temperature, the shorter the diffusion length [7].

All the nodes in the circuit affect the output voltage from each cell. Therefore, full simulation of the chip behavior is very complicated, as each node, in the sensor matrix and at the peripheral circuits is affected by the light because of the carriers long lifetime. The experimentally measured response of a cell in the sensor matrix and its neighbors is shown in Fig. 9. Using this standard process, therefore, makes separation between the cells mandatory. It can be achieved by surrounding each diode with a "guard ring" or putting each diode in a separate well.

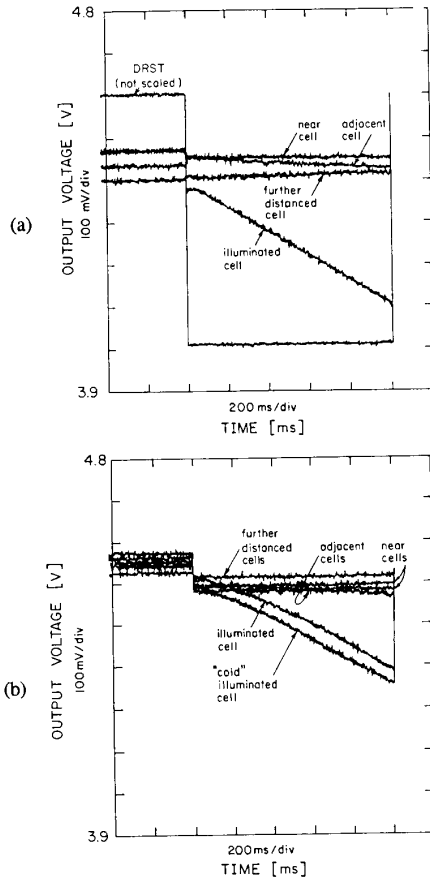


Fig. 8: Test results:
a. At room temperature;
b. After cooling.

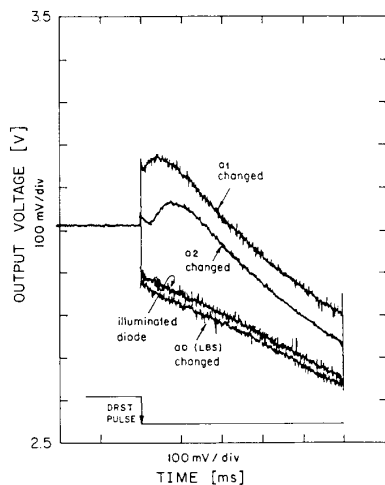


Fig. 9: Measured results in close small cells (at the sensor matrix).

6. Summary

We have described the design and test of a random access photo diode array sensor. It has been planned for Intelligent Scan applications [4]. The chip fulfilled the basic requirements for random access and independent sampling and reading processes.

The chip architecture resembles Random Access Memory (RAM) design. It consists of R rows and C columns of cells, which can be accessed independently. Each cell consists of a photodiode, a memory capacitor and switching transistors. Several alternative designs of the basic cell were tested, differing with the implementation of the connecting blocks, i.e., with or without buffers. The chosen alternative has a buffer at the second stage, in which the current source transistor is shared between all the column transistors.

A novel chip of 80×80 cells with the preferred configuration was fabricated and tested. The chip was found to operate functionally. However, the results point to drawbacks of the design. The crosstalk was found to be the most problematical, and has to be overcome. This phenomenon has been encountered before and several technological solutions can be found in the literature [6, 8, 9].

However, if one still wants to use a standard CMOS process for the imager, future versions will require more area per cell to protect from crosstalk. For instance, fabricating each photodiode in a different well, or inserting guard rings between the diodes are two possible solutions which are aimed at isolating the sensors from each other.

Acknowledgments

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