Prediction of CMOS APS Design Enabling Maximum Photoresponse for Scalable CMOS Technologies

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***Abstract*—This brief represents the CMOS active pixel sensor (APS) photoresponse model use for maximum pixel photosignal prediction in scalable CMOS technologies. We have proposed a simple approximation determining the technology-scaling effect on the overall device photoresponse. Based on the above approximation and the data obtained from the CMOS 0.5 μm process thorough investigation we have theoretically predicted, designed, measured and compared the optimal (in the output photosignal sense) pixel in a more advanced, CMOS 0.35 μm technology. Comparison of both, our theoretically predicted and modeled results and the results obtained from the measurements of an actual pixel array gives excellent agreement. It verifies the presented scaling-effect approximation and validates the usefulness of our model for design optimization in scalable CMOS technologies.**

***Index Terms*—CMOS active pixel sensor (APS), modeling, photoresponse, technology scaling.**

I. Introduction

Past several years of intensive work, have made active pixel sensor (APS) imagers be considered a viable alternative to charge coupled devices (CCDs) in many application fields. However, in the standard CMOS processes of interest here, there is only a limited choice of photodetector devices. In all reported CMOS imagers, photodetectors were realized by using parasitic elements found in the standard CMOS processes [1], [2]. Relatively low sensitivity to incident light (less than that of CCDs of the same pixel size) reduces the imager efficiency, thereby limiting CMOS APS utilization. Investigations have still to be performed for improving and optimizing APS performance in order to meet dedicated application requirements and to provide designers with better control within the existing technology process boundaries. It appears as important to acquire experimental data concerning parameters affecting electro-optics performance, mainly responsivity, resolution and sensitivity to incident light.

It was recently shown [3] that for any potential pixel active area shape in a particular technology process, a reliable estimate of the degradation of image performance is possible, so that the tradeoff between conflicting factors, such as integration photocarriers and conversion gain, could be compared per each pixel design for optimum overall sensor performance. In this brief, we extend the presented analysis and consider the technology-scaling effect on the device photosensitivity. Based on thorough study of the experimental data acquired from several pixel chips fabricated in two different processes, i.e., standard 0.5 μm and standard 0.35 μm CMOS processes, we show the efficacy and the expediency of our photoresponse model (that is summarized in Table I) for scalable CMOS processes.

II. CMOS APS Photoresponse Prediction

Figs. 1 and 2 show two subsets of pixels of rectangular and square shapes, with decreasing photodiode active area dimensions, fabricated in a standard CMOS 0.5 μm process, respectively.

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TABLE I
THE PHOTORESPONSE MODEL, AFTER [3]

$$\frac{V_{out}(\lambda)}{N_{p\lambda}} = (\text{integration photocarriers} \times \text{conversion gain}) = \frac{k_1 A + k_2 P d\left(\frac{S-A}{S}\right)\left(1-\frac{4Pi-P}{8L_{diff}}\right)}{k_3 A + k_4 P}$$

$k_1\ [\mu m^{-2}]$	The number of electrons collected by the unity photodiode area in a time unit
$k_2\ [\mu m^{-2}]$	The number of electrons collected by the "side-wall collecting surface" within the substrate depth
$k_3\ [aF/\mu m^2]$	The bottom capacitance
$k_4\ [aF/\mu m]$	The fringe capacitance
$P_i\ [\mu m]$	The pixel pitch
$d\ [\mu m]$	The depletion depth
$P\ [\mu m]$	The photodiode perimeter
$A\ [\mu m^2]$	The photodiode active area
$S-A\ [\mu m^2]$	The unoccupied photodiode surroundings area within the pixel
$L_{diff}[\mu m]$	The diffusion length
$V_{out}(\lambda)\ [V]$	The pixel signal output for a particular wavelength
$N_{p\lambda}\ [Photons/\sec]$	The photon irradiance

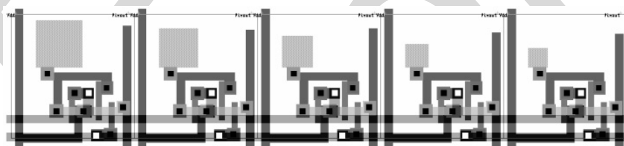

Fig. 1. Subset of square-shaped active area pixels (CMOS 0.5 μm technology, 14 μm pixel pitch) with decreasing (photodiode) dimensions. The photodiode areas vary between 40 μm^2 -5.5 μm^2, and their perimeter varies between 23 μm -9.3 μm, after [3].

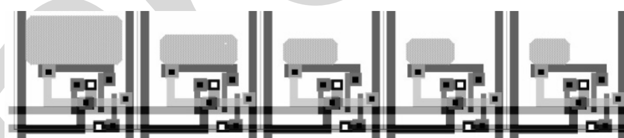

Fig. 2. Subset of rectangular-shaped active area pixels (CMOS 0.5 μm technology, 14 μm pixel pitch) with decreasing (photodiode) dimensions. The photodiode areas vary between 63–13 μm^2, and their perimeter varies between 34–15.5 μm.

Figs. 3 and 4 show the comparison between the corresponding measured and modeled output curves for both sets for several wavelengths lighting. The curves share the same behavior; such that Fig. 3 displays a pronounced maximum response location, while in Fig. 4 the measured curves trend to an extremum.

The photoresponse model presented in [3] and summarized in Table I enables the extraction (by functional fitting) of the unity "main area" (k1) and unity "periphery" (k2) contributions to the output signal (of the measured curves in Fig. 3) at each wavelength, and by that the analysis and modeling of the pixels behavior.

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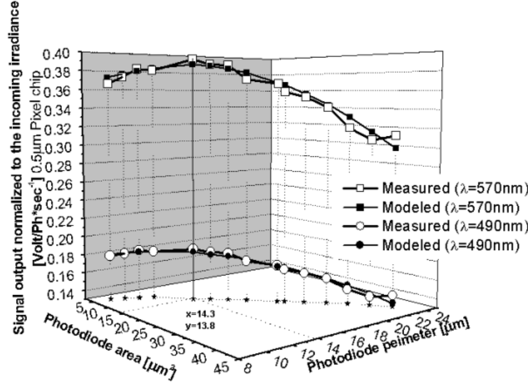

Fig. 3. Comparison of the modeled and the measured results obtained for the square active-area pixels presented in Fig. 1 (CMOS 0.5 μm technology) for two different wavelengths. The geometry of the pixel enabling maximum photoresponse is indicated, after [3].

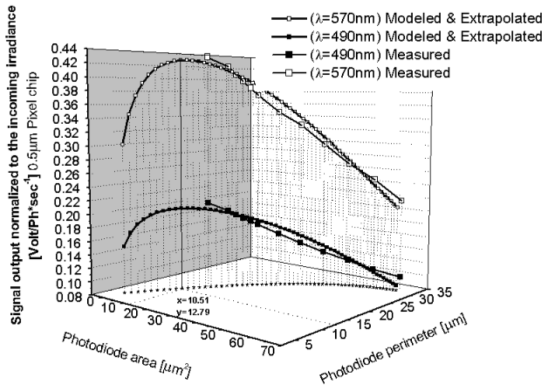

Fig. 4. Comparison of the modeled and the measured results obtained for the rectangular active-area pixels presented in Fig. 2 (CMOS 0.5 μm technology) for two different wavelengths. Model extrapolation envisages the optimal pixel existence and location, i.e., it points out the photodiode area and perimeter corresponding to the pixel enabling maximum photoresponse.

For a certain process, the combination of the above contributions remains invariable for all pixels (i.e., they are independent of the photodiode shape and size) at a certain wavelength exposure [3]. It enables the prediction and the revelation of the maximum response pixel for any (different) photodiode geometry without its realization (in a test chip etc.) based on the specific process and design parameters knowledge only. The extrapolation of the modeled function for the rectangular pixels (Fig. 2), envisages the pixel enabling maximum photoresponse (see Fig. 4); hence, the model theoretically predicts its existence and exact geometrical dimensions, which enable the use of that specific design in applications requiring (for some reason, e.g., the additional logic elements in design) the rectangular photodiode shape.

We have examined the total "main area" and the total periphery contributions to the output signal separately as a function of the photodiode dimensions change. With the dimensions decrease the "main area" contribution scales down, while the periphery contribution scales up, such that their interception occurs exactly at the point where the maximum output signal is predicted by extrapolation (Fig. 4), for the particular CMOS 0.5 μm process, see Fig. 5.

The overall scaling influence on the device sensitivity is very complicated and depends on a large variety of effecting parameters. An analytical expression, uniquely determining the general scaling trends is not yet developed [4], [5]. We propose a first approximation describing the scaling influence and assume that the ratio between the unity "main area" and the unity "periphery" contributions has a slight

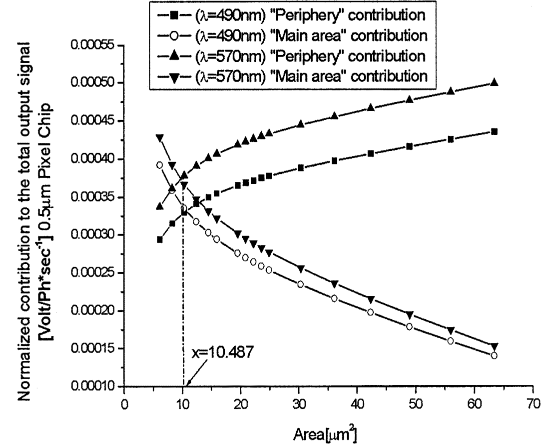

Fig. 5. Total "main area" and "periphery" contributions to the output signal as a function of the photodiode dimensions change for the 0.5 μm CMOS pixel set presented in Fig. 2. The interception occurs exactly at the point where the maximum output signal was predicted by extrapolation in Fig. 4, thus confirming that result.

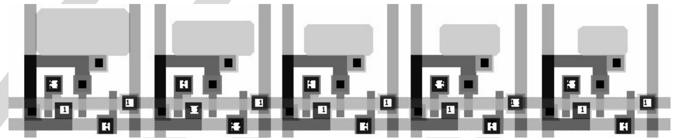

Fig. 6. Subset of rectangular-shaped active area pixels with decreasing photodiode dimensions (CMOS 0.35 μm technology, 7 μm pixel pitch). The photodiode areas vary between 13.4–4.3 μm^2, and their perimeter varies between 15–8.1 μm.

upward trend, mostly through the reduction of mobility and lifetime with increasing doping levels, and shrinkage of the depletion widths. Indeed, under strong absorption conditions where the diffusion coefficient $\alpha(\lambda)$ and the diffusion length L_n both are much smaller than the substrate width, the photocurrent density through diffusion in the substrate can be derived [5] as $J_{ph} = q\Phi/[1 + 1/\alpha(\lambda) \cdot L_n]$, where Φ is the photon flux entering the quasineutral p-substrate region and q – the electron charge. Thereby with technology downscale, the unity "periphery" contribution to the output signal decreases. The depletion width shrinkage means that carriers are collected more through the bottom facet of the depletion region rather than through its lateral facets, intensifying therefore the relative "main area" contribution. Note, in addition, that for advanced processes the junction depth is small in comparison to the absorption depth, such that most photocarriers are collected through the bottom depletion facet [3]. Based on the above assumption and using the process data and the results extracted from the 0.5 μm chip (the coefficients k_1 and k_2), determining the unity "main area" and the unity "periphery" contributions for each particular wavelength), it is possible to determine the coefficients k_1 and k_2 for the more advanced scalable CMOS 0.35 technology. We predict that

$$\frac{k_1}{k_2}\Big|^{570\ \mathrm{nm}}_{\mathrm{CMOS}\ 0.35\ \mu\mathrm{m}} \approx \frac{k_1}{k_2}\Big|^{570\ \mathrm{nm}}_{\mathrm{CMOS}\ 0.5\ \mu\mathrm{m}} \cdot \left(\frac{d_{\mathrm{CMOS}\ 0.5\ \mu\mathrm{m}}}{d_{\mathrm{CMOS}\ 0.35\ \mu\mathrm{m}}}\right) \cdot \left(\frac{L_{n_{\mathrm{CMOS}\ 0.35\ \mu\mathrm{m}}}}{L_{n_{\mathrm{CMOS}\ 0.5\ \mu\mathrm{m}}}}\right) \approx 1.12$$

$$\frac{k_1}{k_2}\Big|^{490\ \mathrm{nm}}_{\mathrm{CMOS}\ 0.35\ \mu\mathrm{m}} \approx \frac{k_1}{k_2}\Big|^{490\ \mathrm{nm}}_{\mathrm{CMOS}\ 0.5\ \mu\mathrm{m}} \cdot \left(\frac{d_{\mathrm{CMOS}\ 0.5\ \mu\mathrm{m}}}{d_{\mathrm{CMOS}\ 0.35\ \mu\mathrm{m}}}\right) \cdot \left(\frac{L_{n_{\mathrm{CMOS}\ 0.35\ \mu\mathrm{m}}}}{L_{n_{\mathrm{CMOS}\ 0.5\ \mu\mathrm{m}}}}\right) \approx 1.07$$

where d is the depletion depth.

IEEE Proof

Consider a set of pixels of a rectangular photodiode shape designed according to the CMOS 0.35 μm design rules and obeying the same mathematical guidelines as the pixels presented in Fig. 2. An example subset of these pixels is shown in Fig. 6. Note that all the pixels share a common, traditional three-transistor type readout circuitry, enabling behavior identification of different pixel types, transistors W/L was scaled 1.5 times from CMOS 0.5 μm to CMOS 0.35 μm.

We use the above predictions for the revelation of a pixel enabling maximum response. In Fig. 7, the total "main area" and the total "periphery" contributions interception point envisages the maximum photoresponse pixel geometry for the pixels set designed and fabricated in the more advanced, i.e., CMOS 0.35 μm technology design (presented in Fig. 6).

Fig. 8 shows the comparison between the corresponding measured and theoretically modeled (based on handy processes and designs data) output curves for several wavelengths lighting where an obvious maximum response geometry is indicated. Note that the modeled function reaches its maximum exactly at the point marked by the measurements; moreover, the values obtained by the measurements for the contributions ratio; $k_1/k_2|^{570\text{ nm}}_{\text{CMOS } 0.35\ \mu\text{m}} \approx 1.13$, and $k_1/k_2|^{490\text{ nm}}_{\text{CMOS } 0.35\ \mu\text{m}} \approx 1.068$ are similar to our theoretical results, and the maximum occurs exactly at the previously predicted interception point (Fig. 7).

The described result is obtained for the 0.35 μm CMOS design based only on the available design and process data and the parameters extracted from the 0.5 μm design, i.e., there was no need for the actual 0.35 μm test chip investigation, such that the optimum geometry, i.e., the pixel enabling the maximum photoresponse was predicted theoretically, based on the investigation results obtained from older process data and scaling considerations only. Thereby, the theoretically obtained prediction is confirmed by the measurements.

III. CONCLUSION

In this brief, we bring out clearly the possibility of a theoretical prediction for a design enabling maximum output signal extraction (for any potential photodiode shape), based on handy process and design data, for different scalable CMOS technologies.

We ratify that first approximation determining the technology-scaling effect expands our photoresponse estimation model [3] field of applicability and enables its use as a predictive tool for design optimization per each potential application in scalable CMOS technologies. Note that since this is the first, simplest model giving a quantitative theoretical value for the pixel photoresponse in various CMOS technologies, further model enhancements are expected to follow.

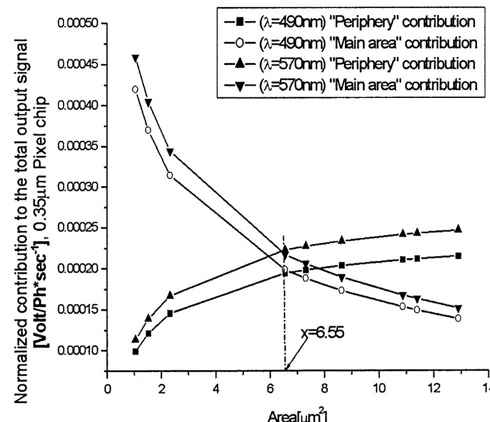

Fig. 7. Total "main area" and "periphery" contributions to the output signal as a function of the photodiode dimensions change for the 0.35 μm CMOS pixel set presented in Fig. 6. Note that this result is obtained theoretically, based on the results analysis obtained from an older 0.5 μm CMOS process and scaling considerations only.

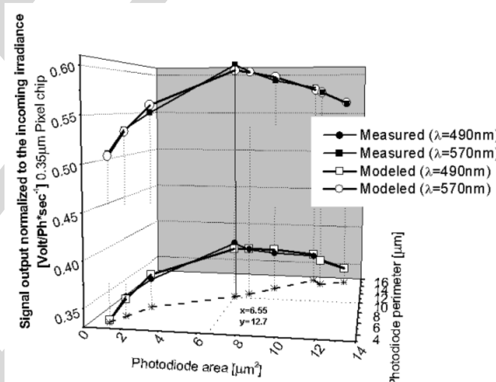

Fig. 8. Comparison of the modeled and the measured results obtained for the pixels presented in Fig. 6 (CMOS 0.5 μm technology) for two different wavelengths. The geometry of the pixel enabling maximum photoresponse is indicated. The maximum occurs exactly at the interception point indicated in Fig. 7, i.e., the theoretically predicted result was confirmed by the measurements.

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REFERENCES

[1] *CMOS Imagers Course Notes*, Ben Gurion Univ., Israel, 2000.

[2] A. Moini, "*Vision chips or seeing silicon*," Univ. Adelaide, Centre for High Performance Integrated Technologies and Systems, 1997.

[3] I. Shcherback and O. Yadid-Pecht, "Photoresponse analysis and pixel shape optimization for CMOS active pixel sensors," *IEEE Trans. Electron Devices, Special Issue on Solid-State Image Sensors*, vol. 50, pp. 12–19, Jan. 2003.

[4] H. Wong, "Technology and device scaling considerations for CMOS imagers," *IEEE Trans. Electron Devices*, vol. 43, pp. 2131–2142, Dec. 1996.

[5] T. Lule, S. Benthien, H. Keller, F. Mutze, P. Rieve, K. Seibel, M. Sommer, and M. Bohm, "Sensitivity of CMOS based imagers and scaling perspectives," in *IEEE Trans. Electron Devices*, Nov. 2000, vol. 47, pp. 2710–2122.