

ADAPTIVE MULTIPLE RESOLUTION CMOS ACTIVE PIXEL SENSOR

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ABSTRACT

A smart image sensor with adaptive multiple resolution ability is presented. This sensor is based on the Quadtree Decomposition algorithm, which decomposes an image into square homogeneous regions. After the image is segmented, only the value of the block and its size are stored or transmitted. On chip implementation can solve the information bottleneck problem by reducing the amount of data for transmission. Good compression results can be achieved for scenes with predominant background. The algorithm is implemented on chip in a mixed signal, column parallel architecture in 0.35 μ m 4M2P n-well TSMC CMOS technology available through MOSIS. Typical power dissipation for the test chip with 32x32 pixels is 70mW at VDD = 3.3V.

1. INTRODUCTION

Fast development of active pixel sensors and different pixel architectures enable smart implementations of various image-processing algorithms. Among these are image sensors for image compression and resolution reduction. In [1], an image sensor with an analog 2-D DCT is presented. An architecture for scene change detection was proposed by Aizawa et al. [2] - with this architecture only the moving areas are encoded. Various architectures for variable resolution implementation were also proposed [3-9]. Panicacci et al. [3] proposed resolution reduction via charge sharing on a capacitor bank. Multiple capacitors are added to the chip in order to store signal from multiple rows of the sensor. In [4] a passive switch-capacitor circuit is used for pixel averaging. The main disadvantage of this design is the large pixel that incorporates additional capacitors for sample and hold. The same disadvantage exists in [5]. Averaging is performed inside the sensor array. The approach presented in [6] uses currents for averaging. In [7] multiple resolution is achieved by integrating the "Signal" and "Reset" separately from different rows. In this presented sensor, as in all previously presented imagers, the capability of changing resolution is enabled only in a uniform way for the whole sensor or for the defined regions of interest through external control. Sensors where windows of higher resolution can be concentrated on the objects in the scene are presented in [8] and [9]. All the image sensors mentioned above could solve the bottleneck transfer problem by significantly reducing the information needed for

transmission. At the same time they do not take into account the scene complexity.

The approach proposed here enables achieving multiple resolutions for different parts of the image that are driven by the image content, while the decisions concerning the resolution in a particular location are made by the circuitry implemented in the sensor periphery. The proposed sensor can be of use in low cost digital cameras, Internet, cellular telephones, etc. A useful feature of the algorithm is that variable compression rates can be achieved.

2. QTD ALGORITHM

The Adaptive Multiple Resolution imager presented in this work is based on the Quadtree Decomposition (QTD) algorithm [10]. It has a simple structure and can be implemented in analog/digital hardware. The algorithm works as a tree. An image is partitioned into square blocks. If a pixel with minimal value and a pixel with a maximal value, belonging to the block, do not lie within a prespecified interval (min/max criterion), the block is further divided into four sub blocks. This process continues till all blocks meet the min/max criterion. An example for one block of 8x8 pixels is shown in Fig. 1. After the image is partitioned into blocks it is enough to send/store only one pixel value from each block with additional information about the size of the block. An example of the QTD algorithm applied to the Airplane image is shown in Fig. 2. As can be seen from this example the algorithm has good compression results for an image with a predominant background (more than 10:1). Aliasing effects can be minimized by choosing a smaller threshold or by taking an average of pixel values, at the expense of more blocks used for the representation.

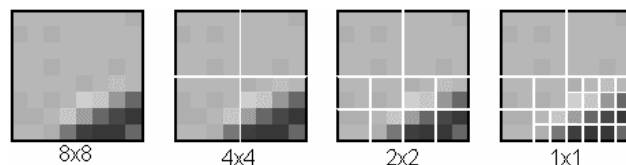


Fig. 1. QTD - blocks formation example description

The main disadvantage of the algorithm is that an image with a large amount of small features can enlarge the image size. This is due to the additional bits required for the block size encoding.

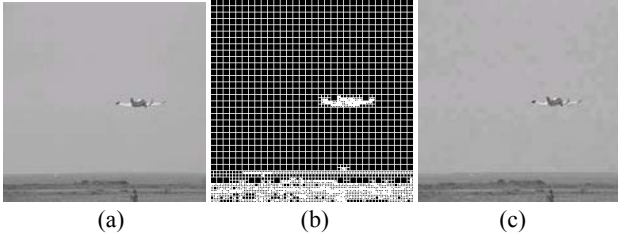


Fig. 2. QTD simulation example (maximal block 8x8):
 (a) original image, (b) block partitioning, (c) restored image

3. CHIP ARCHITECTURE AND CIRCUITS

3.1 Chip architecture

The original algorithm is adapted to suit hardware implementation and a maximum block size of 4x4 pixels is used. All computations are started from a minimum sized block of 2x2 and then the block size conditionally increases to 4x4.

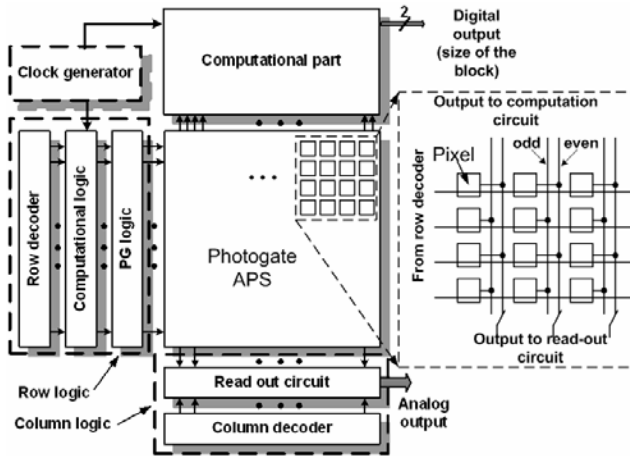


Fig. 3. Chip architecture description.

The chip is composed of five main parts: the photogate active pixel sensor (APS), the row logic, the column logic, the computational circuit and the clock generator circuit. The general architecture of the chip is shown in Fig. 3. The row logic allows simultaneous selection of two rows. The computational circuit is the main part of the chip, it is responsible for block computation and generation of code bits.

Photogate pixels [11] are used in the sensor, since an intermediate node for multiple readout is required, and are organized as shown in Fig. 3, with two output lines per column. This structure allows the processing of two rows of pixels at the same time. The array has two modes of operation, one for computation, where two rows can be selected simultaneously, and the other for read-out where only one row is selected.

3.2 Computational part - architecture

The architecture of the computational part is shown in Fig. 4. It has a modular structure and is organized in a column parallel

manner. It consists of five main parts: a sample and hold (S/H) circuit, winner take all (WTA) and loser take all (LTA) circuits, comparators, memory and digital output logic.

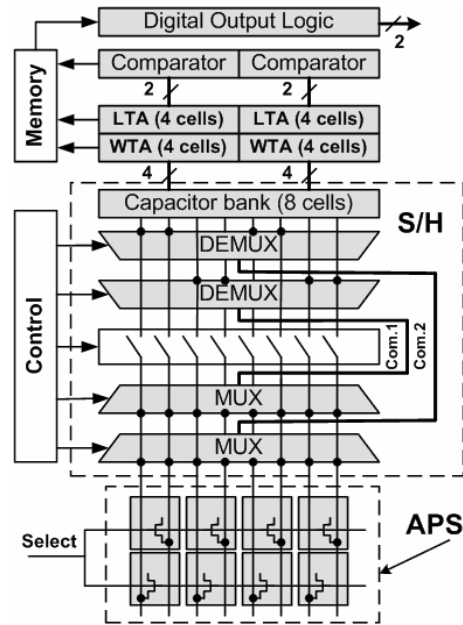


Fig. 4. Computational part architecture.

A combination of switches in the S/H part allows charging any capacitor (out of eight) by the signal from the pixels.

The min/max criterion can be realized in hardware by the WTA/LTA and comparator circuits. The WTA/LTA circuits here are four-input circuits implemented with current steering cells based on [12]. Outputs of the WTA and LTA circuits are connected to a digital memory that stores the coordinates of the winner and the loser.

The comparators have a variable threshold that enables adaptation for different scenes and for the desired quality of the compressed image. The results of the comparison are also stored in the memory.

The digital output logic is the part that generates the 2 bit output for the block size, on the basis of the information stored in the digital memory.

3.3 Computation operation

The general clock diagram is shown in Fig. 5. Simultaneous readout and computation are used. Only "Select" signals for 8 rows and the "Sample Signal" / "Sample Reset" signals are shown. The "Select" signals differ from those used in the conventional sensor because the signal is used a few times for computation and readout. For readout information from the pixels, "Select" exists only when the signal is sampled (time t1 in Fig. 5). When the signal is muxed out from the read-out circuit (time t2 in Fig. 5), we have enough time to compute. Time t2 is used for computation of the next group of four rows.

Clocks numbered from 1 to 10 are computational clocks and allow multiple sampling and block size computation.

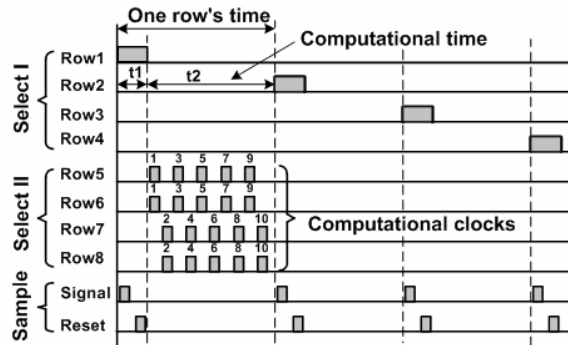


Fig. 5. The clock waveforms implemented.

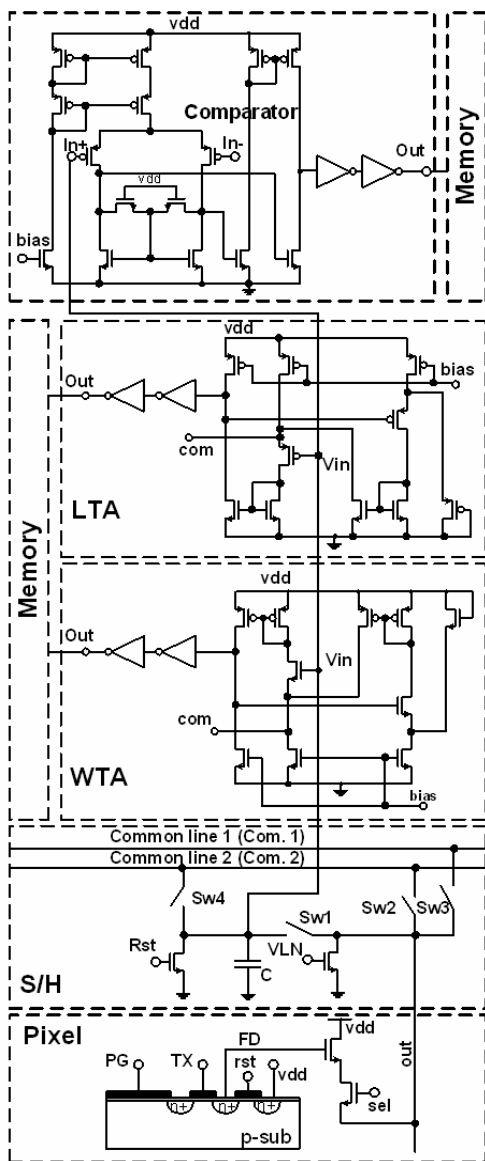


Fig. 6. One column of the computational part

3.4 Circuit parts

One column of the computational part is shown in Fig. 6. A signal from the pixel is sampled by the S/H circuit to the appropriate capacitor C (see S/H part in Fig. 6). A combination of switches ($Sw1-Sw4$) allows access to any capacitor from any pixel from four columns (this property is required for winner and loser comparison). The signal from the capacitor enters the WTA, LTA and comparator circuits. Only one cell of WTA and LTA circuits is shown in the figure. The full circuit consists of four cells (four columns) connected through common line (com). The comparator inputs have control over the current (not shown in the figure). With this control, variable threshold for comparison can be achieved, which gives the possibility to vary the quality of image compression.

With the help of multiple clocks from the clock generator, outputs of all circuits are sampled to the appropriate memories. On the basis of the information present in the digital memory, the digital output logic (not shown in this figure, see Fig. 4) generates a digital output (2 bit) for the block size.

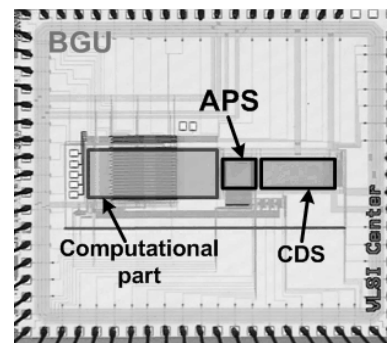


Fig. 7. Test chip microphotograph.

4. RESULTS

Fig. 7 shows the photomicrograph of the imager. Table 1 shows the chip attributes. Chip size is 9 mm^2

Technology	TSMC 0.35 μm
Voltage supply	3.3V
Pixels array	32*32
Pixel type	photogate
Pitch width (pixel)	7 μm
Pitch width (computational)	14.4 μm
Frame scanning frequency	30Hz
Typical power dissipation (computation)	70mW
Fixed pattern noise (FPN)	0.11%
Saturation voltage	1.1 V
Dark current	114 mV/s
Conversion gain	29 $\mu\text{V}/e^-$
Fill Factor	31 %

Table 1. The chip attributes.

Fig. 8 presents experimental results from the test chip. The images at the left are received from the sensor after a correlated double sampling (CDS) circuit. The images at the right are received from the digital output of the chip and show the sizes of the selected blocks. The gray level pixel shows the upper left pixel in the block and represents the digital value of the block size. White is for a 4x4 block which is represented by code 11, dark gray is for a 2x2 block – code 10, and light gray is for a 1x1 block – code 01. The central image is a result of division of the left image into blocks. As can be seen from the images, parts with a uniform color (such as background) are not divided into smaller blocks, while at the same time parts which contain details, are divided to 2x2 or 1x1 blocks. In this test chip, some detailed regions are not divided into smaller regions as was expected. This can be partially due to the lack of CDS in the computational part, which causes some variations between the desired and perceived results.

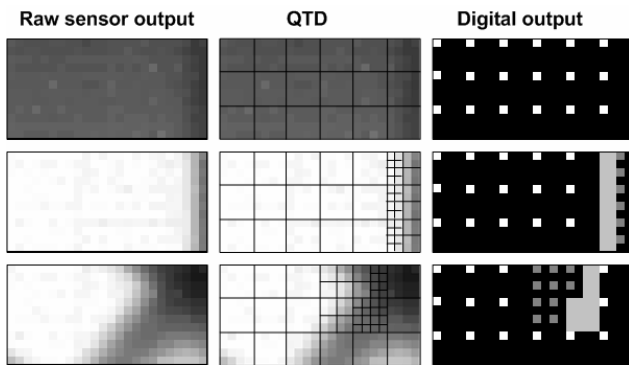


Fig. 8. Experimental results of the computational part applied to various images: left image – image captured by the sensor, right – the digital output from the sensor (white represents 4x4 blocks, dark gray represents 2x2 blocks and light gray represents a 1x1 pixel), center image – the resulted division to the blocks

5. CONCLUSIONS

We have presented here the first implementation of an adaptive multiple resolution sensor. For its realization we have modified an existing Quadtree decomposition algorithm for image compression. As a result, we show an image sensor that transmits a different quantity of information depending on the scene content. Good compression results can be achieved for scenes with predominant backgrounds, since only the object parts are transmitted in full resolution. Variable threshold for the comparison of winners and losers can be achieved manually. This enables adaptation to the scene and to the required image quality.

The imager cons are that a special decoder is needed in order to decompress the transmitted image, and aliasing effects exist due to the block based processing. Also, comparisons here are done without CDS, which adds noise influence to the computation.

Planned future work includes increasing the size of the APS and improving performance of the computational part.

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