

המדריך לסטודנט המתחיל במעבדת VLSI

מסמך זה מהווה היכרות ראשונית עם המערכת והכלים שימשו אותך בעבודה במרכז VLSI. המסמך מחולק ל-2:

חלק א' היכרות עם UNIX

חלק ב' סידור הקבצים ותחילת העבודה עם CADENCE

שימו לב! Cadence הוא שם החברה וVirtuoso הוא שם הכלי בו נשתמש (כפי שMicrosoft הוא שם חברה word הוא כלי)

תכניות שרצות כעת ברקע

היכרות עם UNIX

מסך הפתיחה של מע' הSOLARIS נראה כך:

אייקונים על שולחן העבודה

סל מיחזור

פתיחת חלון יישומים שרצים במערכת ומשאבים פנויים

פתיחת חלון טרמינל

פתיחת סירר הקבצים

פתיחת עורך טקסט

דפדוף בין שולחנות עבודה

נעילה של המחשב – חזרה עם סיסמא בלבד

יציאה Log off

שמירה תמידית של תצוגת הקבצים

סידור מפורטת של הקבצים

שורת הספרייה הנוכחית

מעבר לספרייה שמעל

שמות הספריות

שמות הקבצים

הרשאות כתיבה/קריאה

מי יצר את הקובץ/ספרייה?

ניתן לפתוח טרמינל בספרייה הנוכחית ע"י `file → open Terminal...` או `Ctrl T`
דוגמא: העתקה של קובץ REVISION מחלון ימין לשמאל

לחיצה על סמן עם כפתור העכבר הימני ← פתיחת תפריט אפשריות העתקה/הדבקה
 לחיצה רציפה על כפתור העכבר השמאלי גרירה של הסמן אל החלון הרצוי ועזיבת הכפתור ← העברה
 לחיצה רציפה על כפתור העכבר השמאלי גרירה של הסמן אל החלון הרצוי ועזיבת הכפתור + CTRL ← העתקה

ספריית עבודה:

פתחו את סירר הקבצים והתחילו בספריית העבודה.
 ספריית העבודה שלכם נקראת {user_name}/users/natapp/vlsi/
 כאשר שם המשתמש שלכם הוא {user_name}
 ספריית העבודה מכילה את כל קבצי המידע עליהם תעבדו.
 בספרייה הבאה נמצאים כל קבצי המקור הדרושים לעבודה עם Cadence Virtuoso:
 /usr/cds/TSMC18rf
 לחיצה על Ctrl s תציג את הקבצים המוסתרים המתחילים ב".cdsend"
 בספריית העבודה קיימים הקבצים הבאים:
 cdsenv. קובץ המכיל את הגדרות הdefault של אפשרויות הכלים השונות.
 cadence_setup. קובץ המכיל את הגדרות מיקומי (path) התוכנות השונות של חברת Cadence.

ספריית הפרויקט

בתחילת כל פרויקט, יש לפתוח ספריית פרויקט חדשה בשם הטכנולוגיה איתה תעבדו – לדוגמא "TSMC_018"
 ניתן ליצור את ספריית הפרויקט דרך התפריט הגראפי של סירר הקבצים
 file→New folder...
 לאחר מכן להיכנס לספריית הפרויקט ע"י לחיצה כפולה עם עכבר שמאל.
 בספריית הפרויקט נמצאים הקבצים/ספריות הבאים:
 cds.lib קובץ טקסט המכיל הפניות לספריות העבודה המכילות מידע (הניתן לקריאה בלבד) שבו תשתמשו וגם את
 ספריות העבודה אותם תיצרו, ושבהם תשמרו את המידע שלכם.
 display.drf קובץ טקסט המכיל את צבעי השכבות ב Layout.
 cdsinit. קובץ טקסט הקורא לפונקציות מע' בין היתר גם את לפונקציות יצירת מקשי קיצור הדרך (bindkeys.il)
 .lvs.last.state. קובץ המכיל את ההגדרות של תפריט הLVS של ASSURA
 .drc.last.state. קובץ המכיל את ההגדרות של תפריט הLVS של ASSURA
 assura_tech.lib קובץ טקסט המכיל הפניות לספריות קבצי המידע עבור ביצוע LVS וDRC עבור LAYOUT
 Assura ספרייה המכילה את קבצי המידע עבור ביצוע LVS וDRC עבור LAYOUT

שימו לב: קבצים המתחילים ב".cdsend" הם קבצים מוסתרים.

אם אתם לא רואים אותם ליחצו על CNTRL+S או בתפריט סירר הקבצים View→Show Hidden Files

כעת הכול מוכן להתחלת העבודה עם Cadence Virtuoso

Starting with cadence

Before you start working on cadence you should approach our system administrator.
 Ask him to attach to your account TSMC018RF technology.
 First of all, open the console on the Unix machine.



Then a console window pops up as shown below.

```

Console
Window Edit Options
Sun Microsystems Inc. SunOS 5.7 Generic October 1998
PSC design kit environment set.
CADENCE setup for Solaris done.

+++++
+ /tmp/SoC_v1 : EXIST.
+ FILE .display : NOT CREATED
+ DISPLAY NOT SET
+ Permission is : drwxr-xr-x
+++++

piper ~ SoC_v1$ cd TSMC_018
piper ~ /TSMC_018$ SoC_v1$ icfb&
[1] 8098
piper ~ /TSMC_018$ SoC_v1$ sh: /usr/bin/X11/x1sfonts: not found
  
```

process number

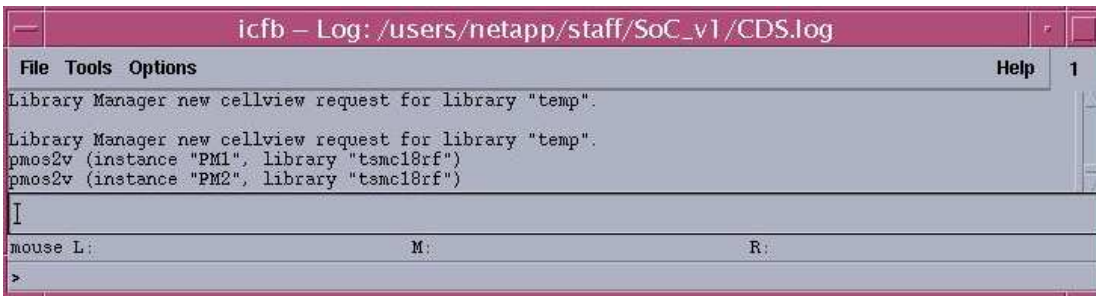
In order to use Cadence tools.

Type “cd TSMC_018” and press ENTER.

Type “icfb&” and press ENTER.

The process number allow you to exit the Cadence tools if it stacked by typing “kill 8098” in console window .

CIW



```

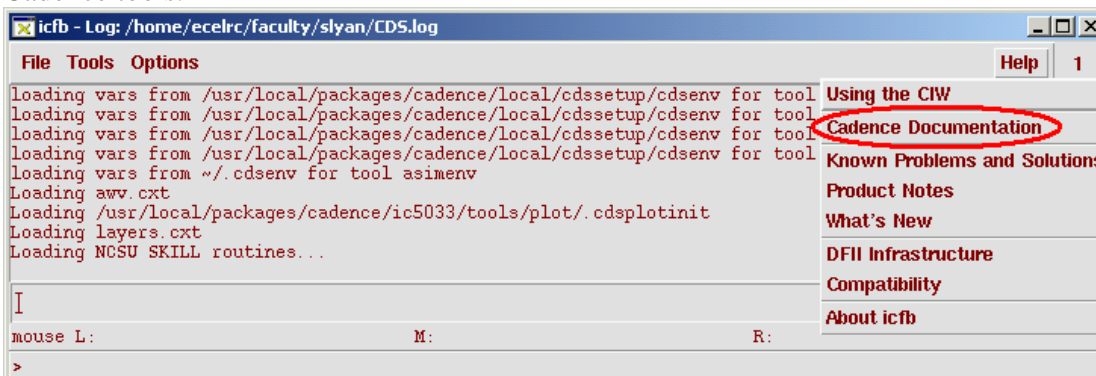
icfb - Log: /users/netapp/staff/SoC_v1/CDS.log
File Tools Options Help 1
Library Manager new cellview request for library "temp".
Library Manager new cellview request for library "temp".
pmos2v (instance "PM1", library "tsmc18rf")
pmos2v (instance "PM2", library "tsmc18rf")
[
mouse L: M: R:
>
  
```

After a short while, a window, called “CIW” (Command Interpreter Window), appears as shown above. CIW displays Cadence log file “CDS.log” stored in your home directory. When you use a specific Cadence tool (e.g. Virtuoso) and run a task (e.g. DRC), most of the times the results will be displayed in CIW. Thus you should check back on this window quite often to know what is happening for the tasks that you have initiated.

Your Cadence designs (schematic, layout, ...) are organized in libraries. You can go to menu “Tools->library manager” to invoke the library manager. The library manager usually automatically starts after CIW appears, thus you may not need to do that.

Cadence document can be invoked by the “Cadence Documentation” through the Help menu of CIW as shown below.

Type “cdsdoc&” on the command Console of UNIX (not in CIW) to read the documents for all Cadence tools.



```

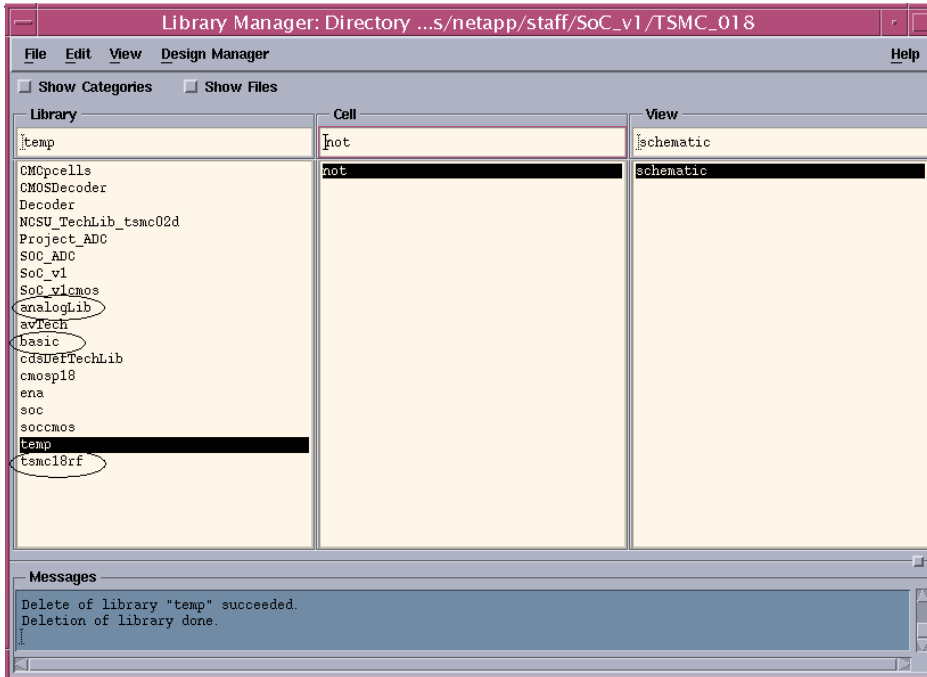
icfb - Log: /home/ecelrc/faculty/slyan/CDS.log
File Tools Options Help 1
loading vars from /usr/local/packages/cadence/local/cdssetup/cdsenv for tool
loading vars from /usr/local/packages/cadence/local/cdssetup/cdsenv for tool
loading vars from /usr/local/packages/cadence/local/cdssetup/cdsenv for tool
loading vars from /usr/local/packages/cadence/local/cdssetup/cdsenv for tool
loading vars from ~/.cdsenv for tool asimenv
Loading awv.cxt
Loading /usr/local/packages/cadence/ic5033/tools/plot/.cdsplotinit
Loading layers.cxt
Loading NCSU SKILL routines...
Using the CIW
Cadence Documentation
Known Problems and Solutions
Product Notes
What's New
DFII Infrastructure
Compatibility
About icfb
[
mouse L: M: R:
>
  
```

The Library Manager

CIW and Library Manager are probably the two most important and most frequently used windows in Cadence tools. CIW shows the log information; Library Manager helps you manage your designs which are generally organized in a number of cells. When you start a design in Cadence for the first time, you have to create a library where you can store your designs. Every library is associated with a technology file that supplies all the color maps, layer maps, design rules, extraction parameters required to view, design, simulate and fabricate your design.

1. Starting Library Manager

The Library Manager usually automatically starts after CIW window appears. In case that the library manager has not started, or accidentally was closed, go to CIW window, click on “Tools->Library Manager”. Library Manager looks like the window in next page.

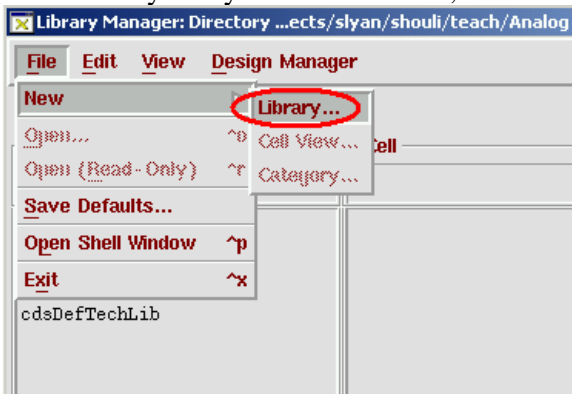


Before you move forward check that the libraries analogLib ,basic and **tsmc18rf** are exist in the library manager.

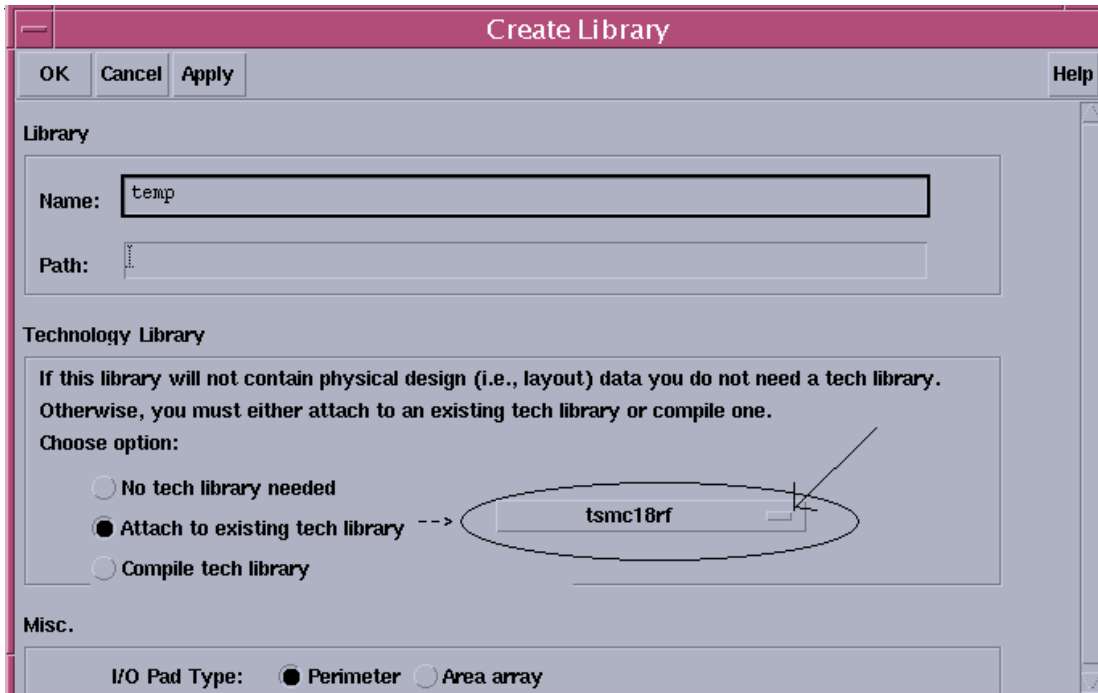
2. Create New Library

In Library Manager window, click on “File->New->Library...”

You will see a dialog window pop up, as shown in the right. At the “Name” field, enter the name of the library that you want to create, in our case “temp”, to store your design cells.



Attach this library to an existing technology (example shown: tsmc 0.18 μm technology) by clicking the radio button “Attach to existing tech library -->” and choosing “other->tsmc18rf”, thus the Cadence tools would know the technology specifics of your design (like SPICE models, DRC rules, ERC rules, etc.) Please do not enter or change any other fields or options.




The library temp will be added to your library manager window (see previous page).











You have not only created a library “temp” of your own, but also included its associated technology library “tsmc18rf” in your library path. By right clicking on the library you have a variety of options :deleting it, check properties of the library, or attaching another technology.

Schematics Using Virtuoso Schematic Composer

At this point, you have created a library (in the example “temp”) to store your design and can start the design process. For a full custom design, the process begins by creating a schematic. Then we simulate this design to verify its functionality and analyze its behavior to optimize the performance. Only after this is done, we will start the layout of the design. There may have up to three ways to initiate a command in Cadence Schematic Composer and Layout Editor, (1) choose a menu from the top menu bar; (2) click a button on the left toolbar of the window, or (3) press a *hot key*. All of above three ways will have the same results. You can choose what like the best. For example, to add an instance, you can choose “Add -> Instance ...” from the menu bar, or you

can click the button  from tool bar at the left side of the window, or, you can simply press the hot key “i” from the key board.

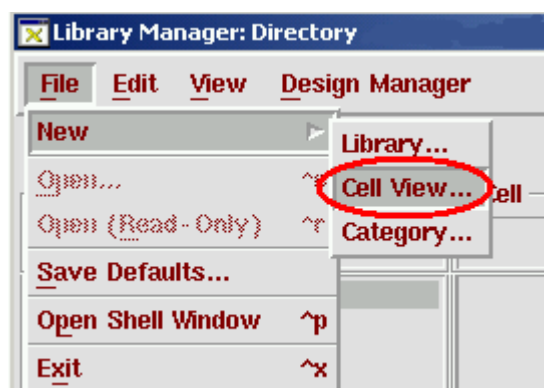
1 .Hot keys, menus, and tool buttons

Tool button	Menu	Hot key	Function
	Design ->Check and Save	F8	Check and save
	Add ->Instance...	i	Add instances
	Edit ->Properties	q	Edit properties
	Add ->wire (narrow)	w	Add wires
	Add ->Wire Name...	l	Label a wire
	Edit ->Delete	DEL	Delete (a pin, label, wire, instance...)
	Add ->Pin...	p	Add a pin
	Edit ->Undo	u	Undo
	Window ->Zoom ->Zoom In	CTRL Z	Zoom in
	Window ->Zoom ->Zoom In By 2	Shift z	Zoom in by 2X
	Window ->Zoom ->Zoom Out By 2	CTRL Z	Zoom out by 2X
	Window ->Fit	f	Fit the schematic

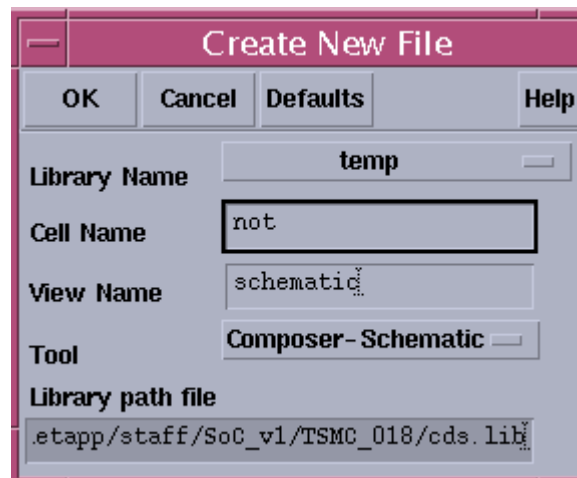
For more hot keys check **appendix a** in the end of a lecture.

2. Create New Schematic

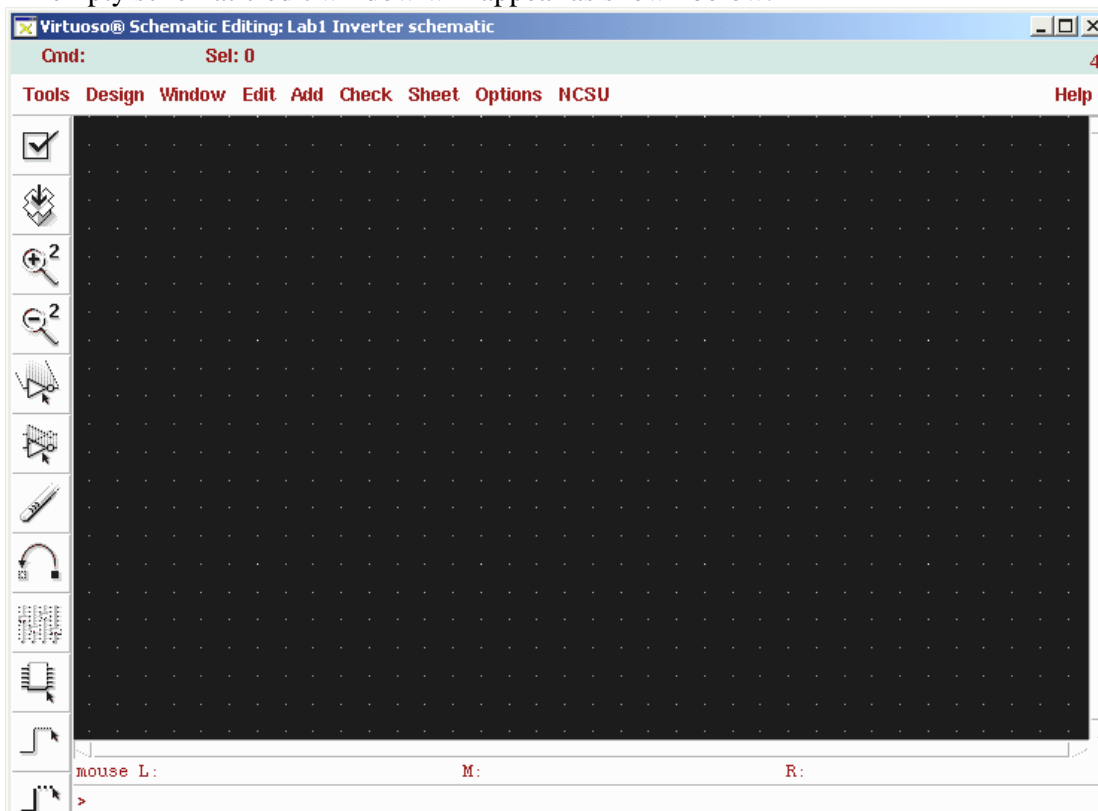
In your Library Manager window, click on the “File->New->Cellview”. A pop-up dialogue box appears.



Click on the library name button and select “temp”. Click on the “Tool” button to select “Composer-Schematic”. The “View Name” will automatically change to “schematic”. Enter the name of the cell you wish to design in “Cell Name”. For this lab, we will design a CMOS inverter, with the cell name of “Not”. Click “OK” after you type in the cell name.




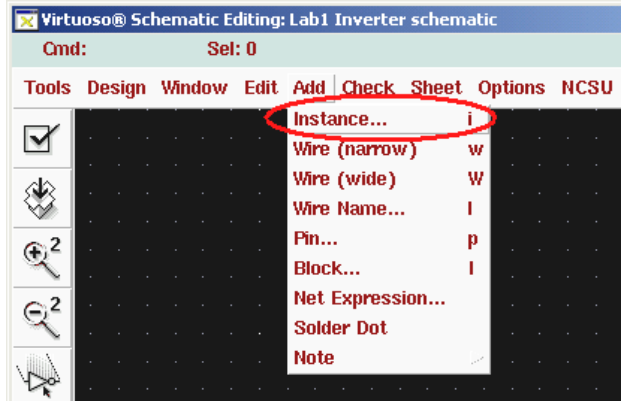
An empty schematic edit window will appear as shown below.



In the following steps, we will learn how to create an inverter in this schematic window.

3. Adding an Instance

To place an instance, e.g. an NMOS device, in your schematic, activate the schematic window, then click on menu “Add->Instance” (or type “i” hot key, or click  on the left side tool bar). The “Add Instance” dialogue box appears together with the “Component Browser” dialogue box. In case the that does not appear, click on the “Browse” button in the “Add Instance” dialogue box to start it.



In “Component Browser” window, click on “Library” multi-selection button and choose “tsmc18rf”. Click on “MOS” and choose “nmos2v” as your NMOS device . To place the instance, activate the schematic window and click the left mouse button to put the instance at the place desired.

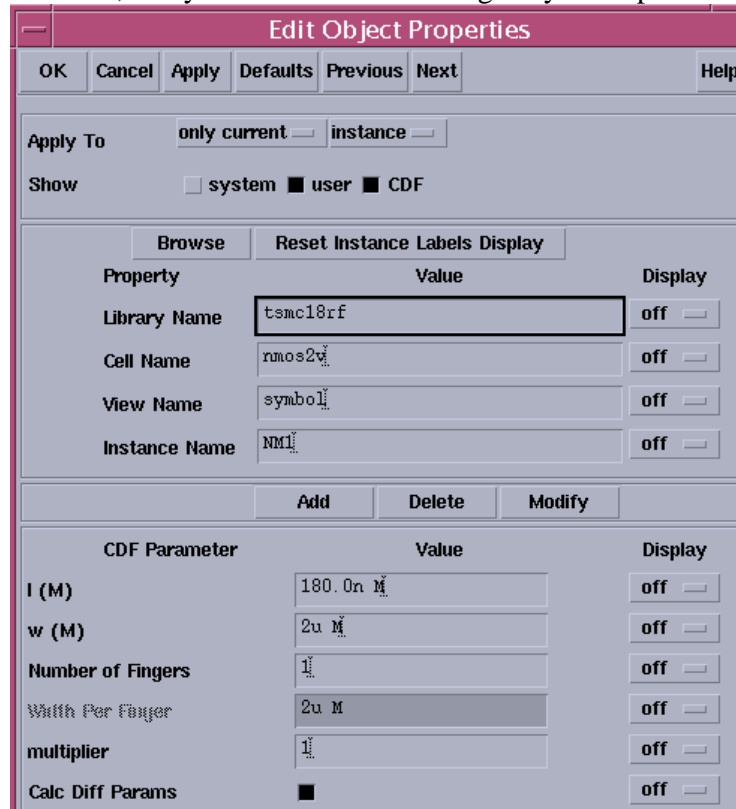


Note in Cadence schematic composers and layout editors, a command will not terminate unless the user cancels it or the user starts a new command. In this case, you can see another instance is ready to be placed right after you placed the first instance. To terminate the current operation (which is “Add Instance” in this case), press **ESC** key on the keyboard. In fact, you can always cancel the current operation in schematic or layout editors by pressing **ESC** key.

In order to place vdd and gnd in “Component Browser” window, click on “Library” multi-selection button and choose “analogLib”. Click on “Sources->Globals” and choose “vdd” and “gnd” .

4. Set The Properties

To set the properties of the instance that you just placed or any object in your schematic or layout design, select the object by clicking on it and then go to “Edit->properties->Object...” (or by typing “q” hot key). An object properties editing form will pop up. The following is the properties window of an NMOS Transistor. Change the “Width”, “Length”, and “Multiplier” properties to desired values, and you do not need to change any other parameters.



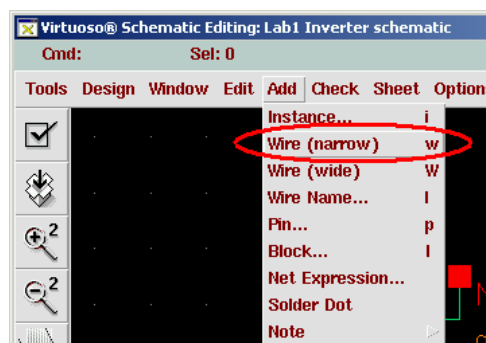
Property	Value	Display
Library Name	tsmc18rf	off
Cell Name	nmos2v	off
View Name	symbol	off
Instance Name	NM1	off

CDF Parameter	Value	Display
I (M)	180.0n M	off
w (M)	2u M	off
Number of Fingers	1	off
Width Per Finger	2u M	off
multiplier	1	off
Calc Diff Params	<input checked="" type="checkbox"/>	off

In a similar manner, we can add an instance of PMOS transistor. Set the properties of the PMOS transistor as, “Width”=2u, “Length”=0.18u, and “Multiplier”=1. Set the properties of the NMOS transistor as, “Width”=1u, “Length”=0.18u, and “Multiplier”=1.

5. Connecting the Instances With Wires

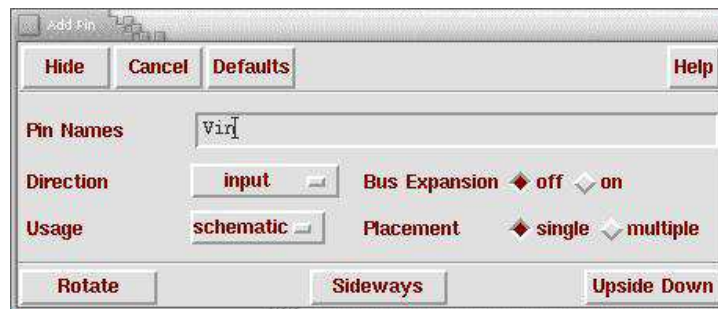
To connect the PMOS and NMOS devices or any other devices, click on “Add->Wire(narrow)” in the schematic window (or type “w” hot key). Click at the terminal where the wire starts, and then click at the terminal where the wire ends, a wire will be automatically added. If you are not satisfied with the automatic wiring, you can remove the wire by press DEL key and reroute it manually. This time, instead of clicking at the terminal where the wire ends directly, you can click the left mouse button whenever you want to change the wire direction.



If you want to stop the wire somewhere instead of connecting it to a terminal, double click your left mouse button and a dangling wire is created. In general dangling wire should be avoided, however, in some cases, for example, if you want to label this wire or add a pin to this wire, a dangling wire makes sense.

6. Create pins

Click on “Add->Pin...” (or type hot key “p”) in the schematic window, the following dialogue box would appear. We have to specify its input/output behavior for each pin. For an input pin, choose the “Direction” to be “input”. Specify the Pin Names (“vin” in the example). Activate the schematic window and click on the left mouse to put the pin on the schematic. Similarly we can add an output pin (Vout in the example) to the output of the cell.



7. Check and save the designs

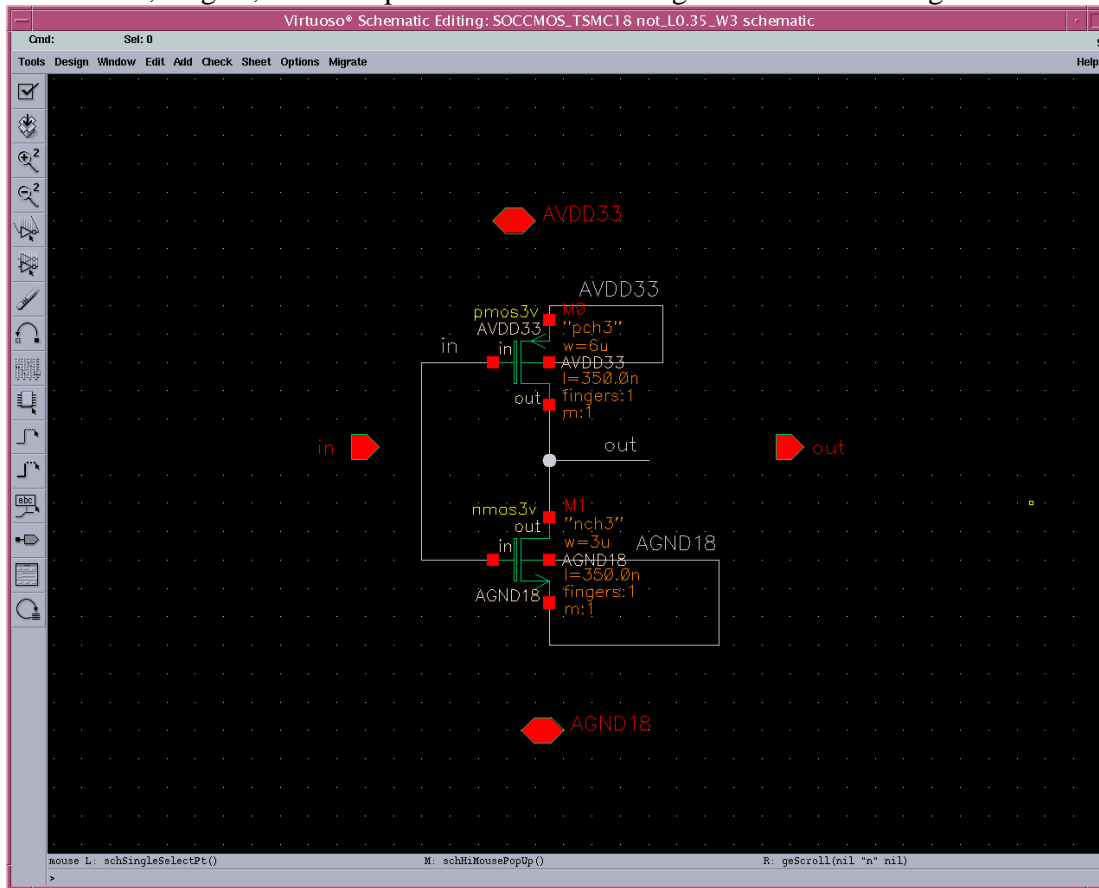
After the design has been completed, click on “Design->Check and Save” to check and save your design. Go to the CIW window to see if there is any error in your design. The following schematic shows the completed design of the Inverter.

```

icfb – Log: /users/netapp/staff/SoC_v1/CDS.log
File Tools Options
Schematic check completed with no errors.
"temp not schematic" saved.
Extracting "not schematic"
Schematic check completed with no errors.
"temp not schematic" saved.
I
mouse L: showClickInfo()           M: schHiMousePopUp()           R: schHiCheckAndSave()

```

Use the widths, lengths, and multipliers of the transistors given in the following screen shot.



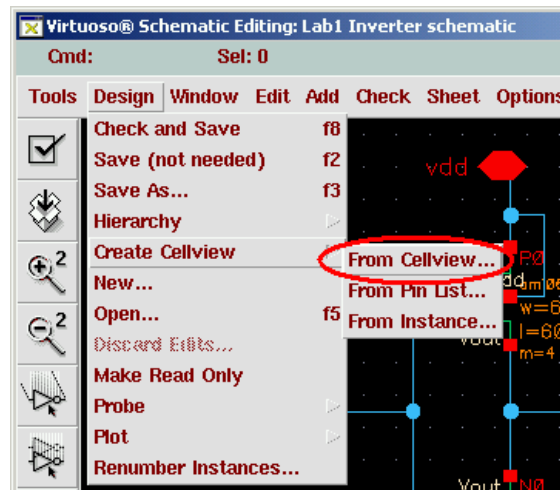
Please note that Cadence automatically labels internal nodes, usually you don't have to explicitly label them.

Creating Symbols

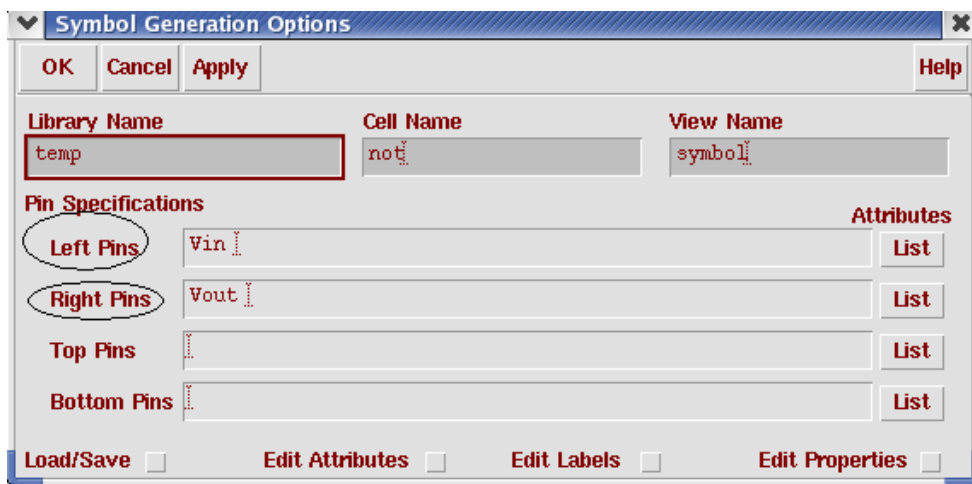
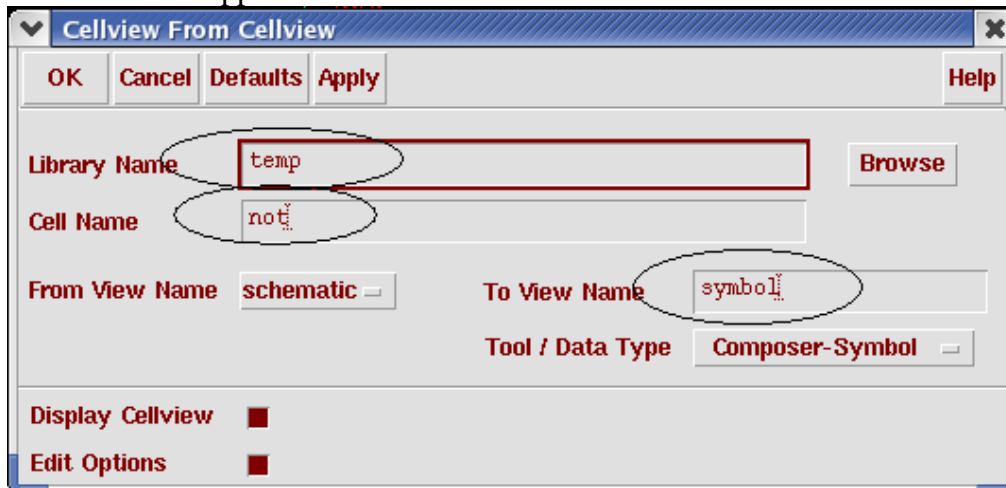
Symbols are useful when the schematic design is done hierarchically. At a higher level of abstraction, we would like to use a symbol to replace the details of a cell. The symbol of a schematic cell should define all the inputs and outputs of that cell.

Create Symbol From a Schematic

Click on "Design->Create Cellview->From Cellview" menu in the schematic edit window, a pop up dialogue box will appear.

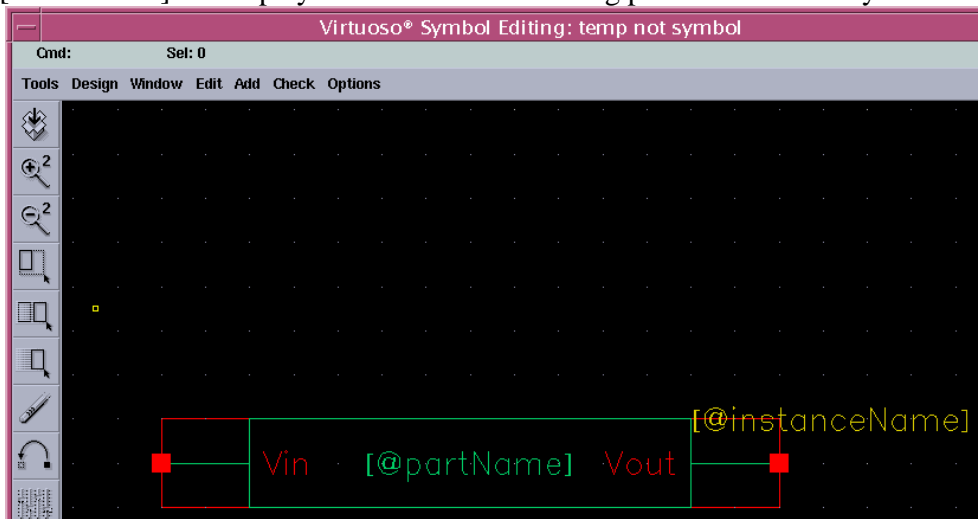




A window will appear:

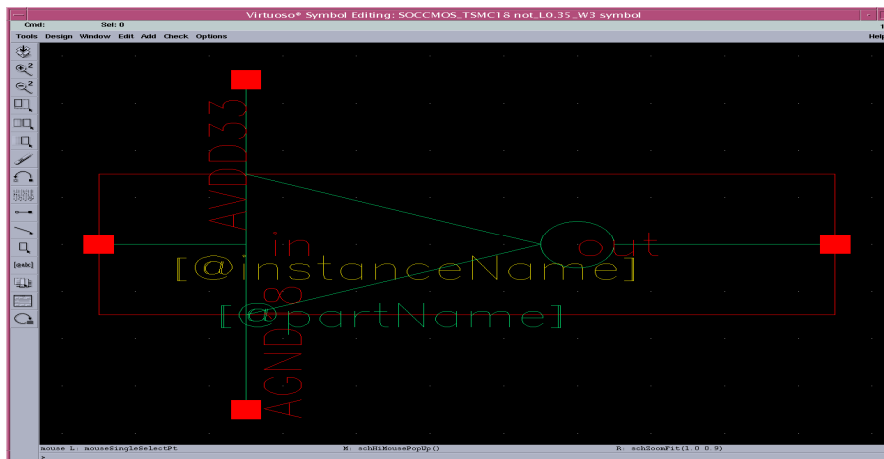


As you see you can define the location of every pin in symbol left/right/top/bottom

We can use the default setup in this window, thus just click “OK”. The symbol edit window will appear that contains a default symbol picture created automatically by Cadence. It has a red box that encloses the green colored inverter symbol. This red box defines the actual size that a symbol will occupy. You can change the size of this box. It is preferred to exactly fit the symbol within the red box. The red square dots indicate the pin connections. [@InstanceName] and [@PartName] are display variables. The following picture shows the symbol.



Choose menu “Add->Shape->Line” or click the tool bar icon , and draw a triangle. Choose menu “Add->Shape->Circle” to add the small circle of the inverter. Move the pins, triangle, and the small circle, if necessary, by select and move them one by one. Resize the red rectangle if necessary by choosing menu “Edit->Stretch” or by clicking the tool bar icon , and stretch one side of the red rectangle. You finally get a symbol that looks like this.



The Analog Environment

The Analog Environment

Now is the Time to use the Analog Environment for the Simulation Purpose. Actually the Schematic that you have previously created is the schematic shown in the problem. You have to slightly modify the schematic now to apply the desired voltages and the currents. The Input Voltage source is now to be specified and the Output is to be measured between the output pin and ground with a capacitor in between the 2 nodes.

Then you will open the Analog Environment and perform actual simulation on the design of the Inverter that you have just built. You have to specify the Outputs that are to be plotted on the Results Browser and you will specify the input source and the time for the Analysis and Observe the results.

Following the procedure to create “not” schematic, create a new schematic "Inverter_tst".

Now add your not gate as an instance to your current schematic.

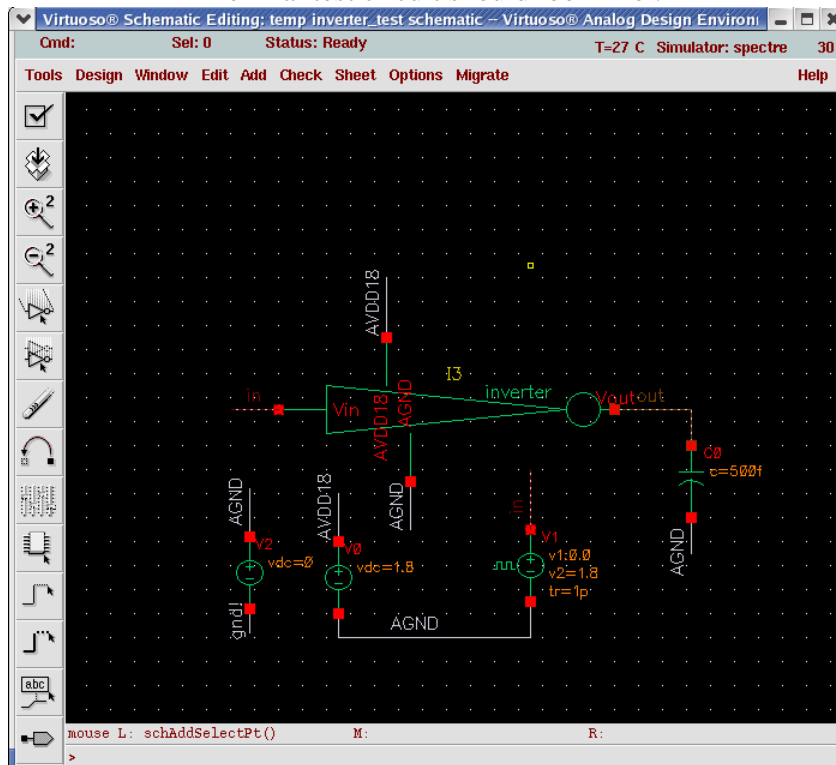
Once you created schematic as a symbol you can always add it as na instance in another schematic. In order to place gnd in “Component Browser” window, click on “Library” multi-selection button and choose “analogLib”. Click on “Sources->Globals” and choose "gnd" . Click on “Passives” and choose "cap" . Give it 500fF value.

Click on “Sources->Independent” and choose "vdc". Give it dc voltage=1.8v value.

Click on "Sources->Independent" and choose "vpulse". Define it like this

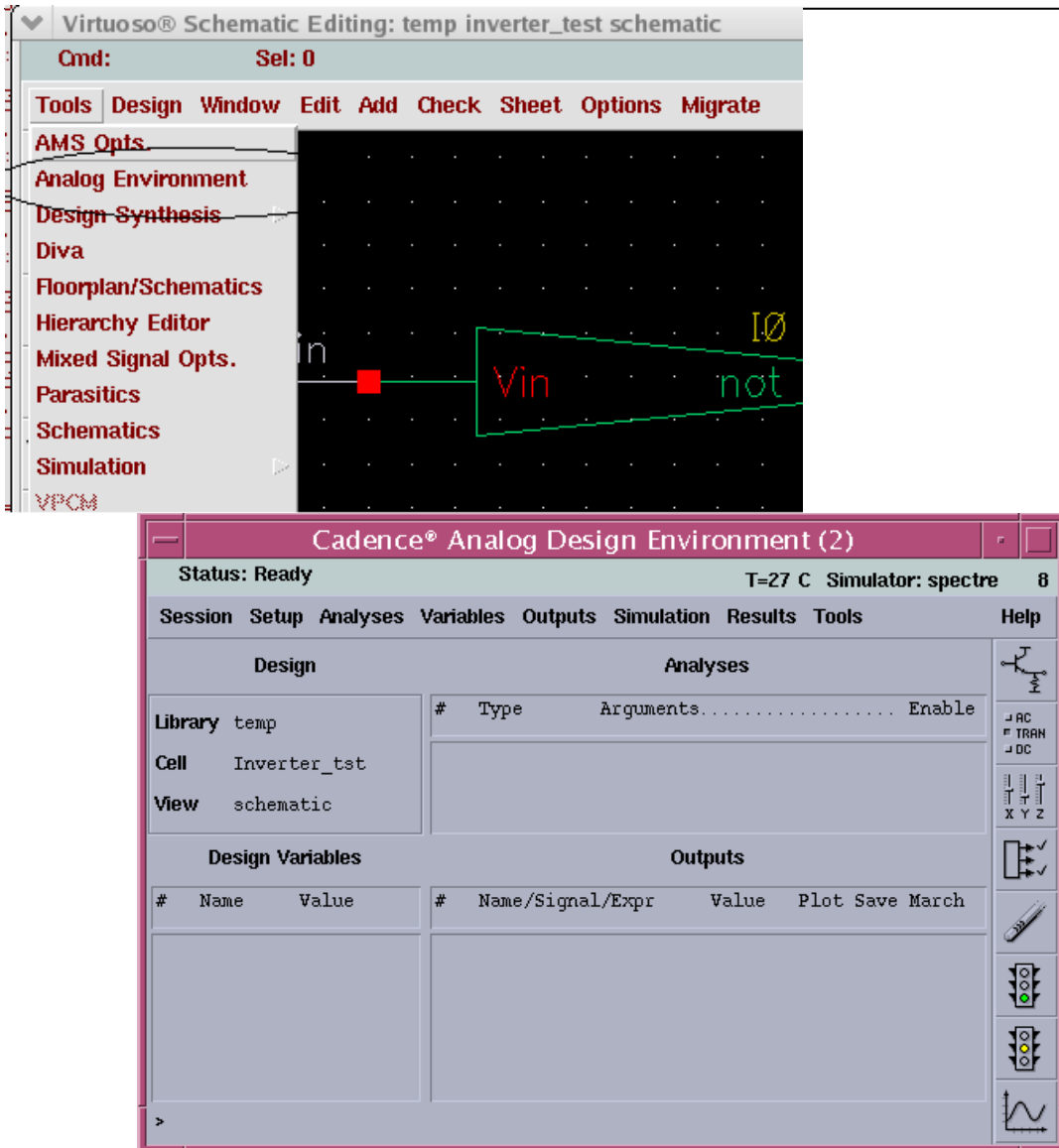
Browse		Reset Instance Labels Display	
Property	Value	Display	
Library Name	analogLib	off	▾
Cell Name	vpulse	off	▾
View Name	symbol	off	▾
Instance Name	v1	off	▾
		Add	Delete
		Modify	
User Property	Master Value	Local Value	Display
IvsIgnore	TRUE		off ▾
CDF Parameter		Value	Display
AC magnitude		off ▾	
AC phase		off ▾	
DC voltage		off ▾	
Voltage 1	0.0 V	off ▾	
Voltage 2	1.8 V	off ▾	
Delay time	0 s	off ▾	
Rise time	1p s	off ▾	
Fall time	1p s	off ▾	
Pulse width	20n s	off ▾	
Period	40n s	off ▾	

The final test circuit should look like :

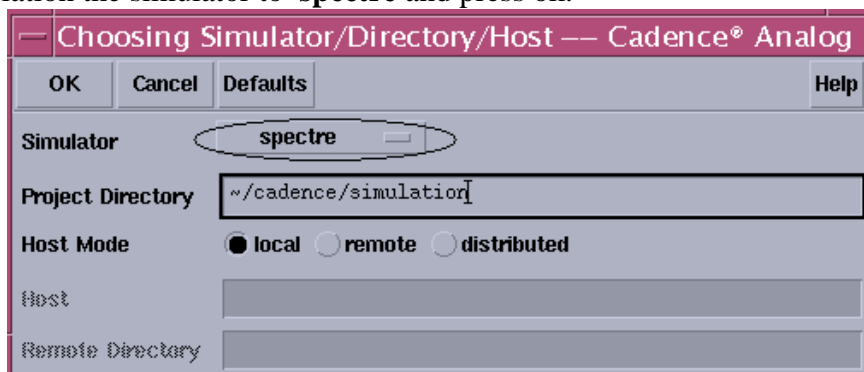


Notice that you do not have to connect the wires physically . In order to connect them It's enough to give them the same name. Also notice that vdd! And gnd! Are global nets because of "!".

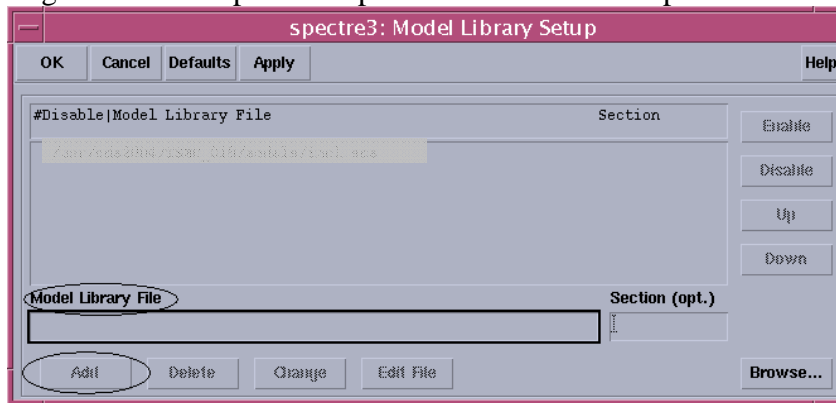
Now, After You have finished completing the schematic it is time to open the Analog Environment in Cadence. In the Schematic Window, go to "Tools->Analog Environment" he following window will pop up.



Before you start simulation enter to setup and choose Simulator/Directory/host.
 For the simulation the simulator to **spectre** and press ok.



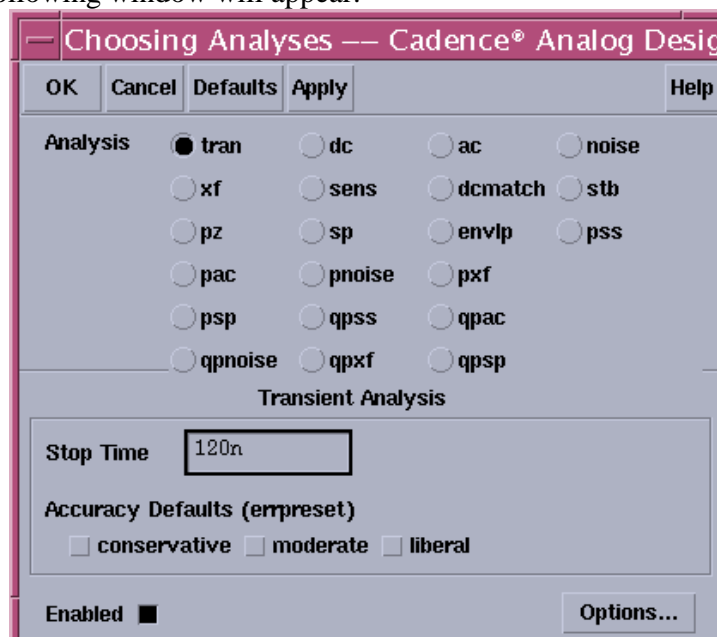
Next from Analog Environment press setup-> model libraries setup



In model library file type `/usr/cds/TSMC_018/models/ incl.scs` and press on the Add button. This stage is necessary for the simulation to work.

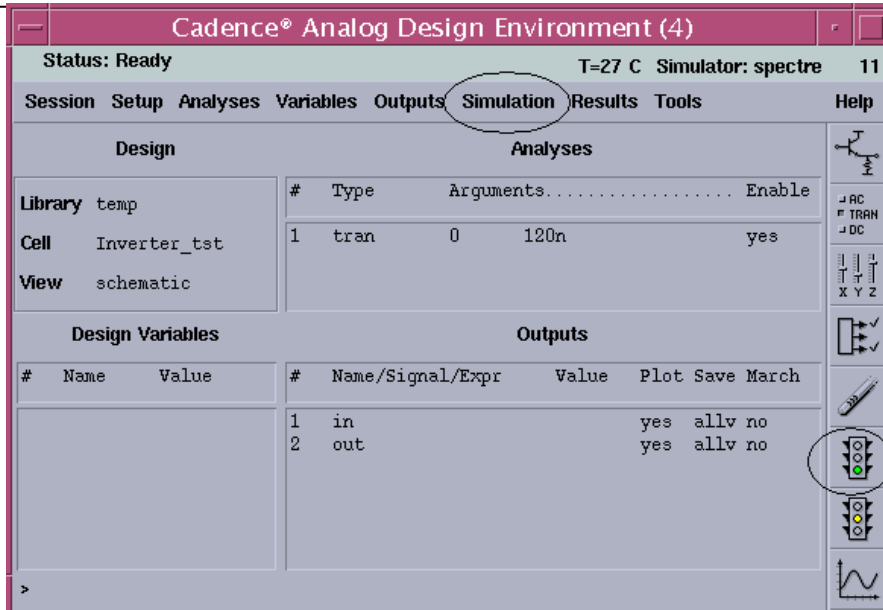
Now you can start simulate.

You need to specify the outputs that you need to view and choose the type of analysis that you are using for your simulation. Go to “Outputs->To Be Plotted->Select from Schematic” and then you are sent to the schematic. Click a wire to select a voltage and a device pin to select a current, when finished hit <ESC>. In our case choose "in" and "out" to be plotted. Then you need to specify the analysis used for simulation. Go to “Analyses-->Choose...”, the following window will appear.



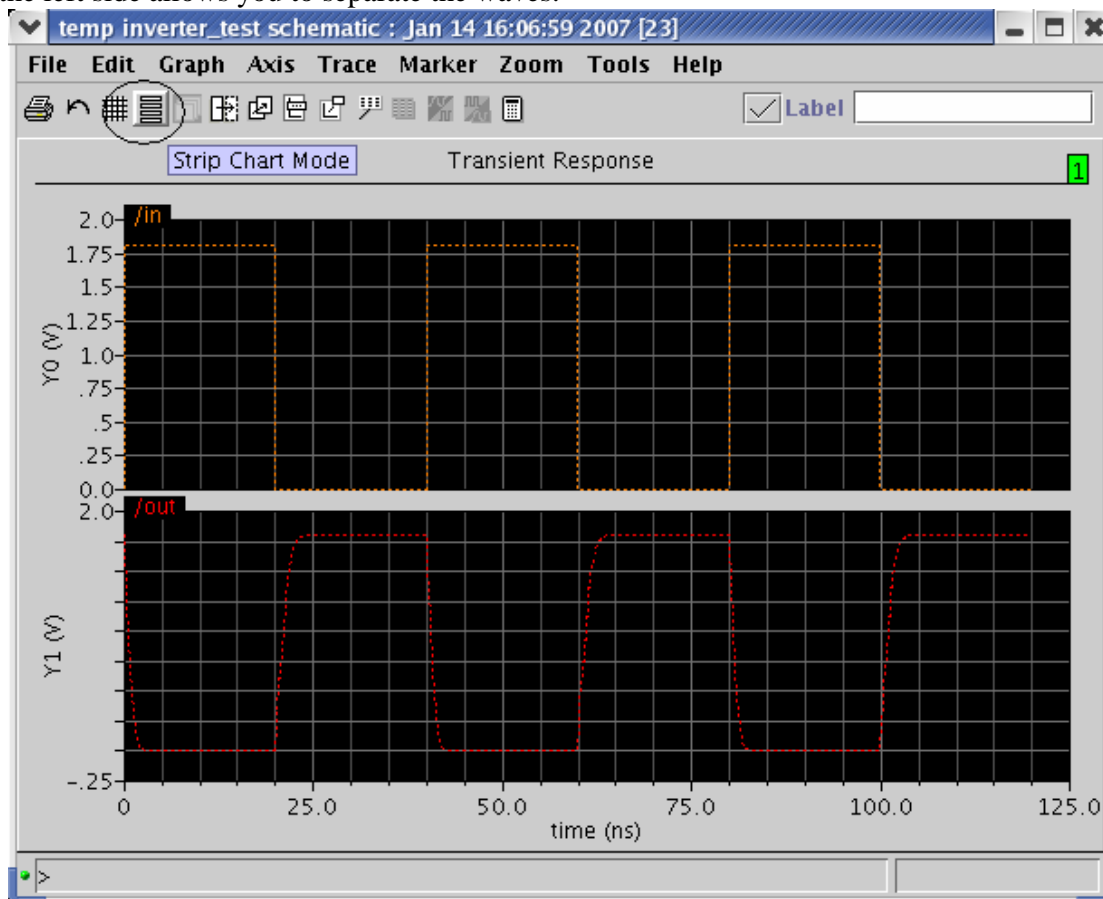
As you can see spectre allow a variety of different analysis but we will choose the most common one. Select the tran (transient) Analysis, and choose Stop Time 120n.

Now it is time for the Actual Simulation. In the Analog Environment window go to “Simulation->Run” or press the icon with green light and spread out and wait for the results.

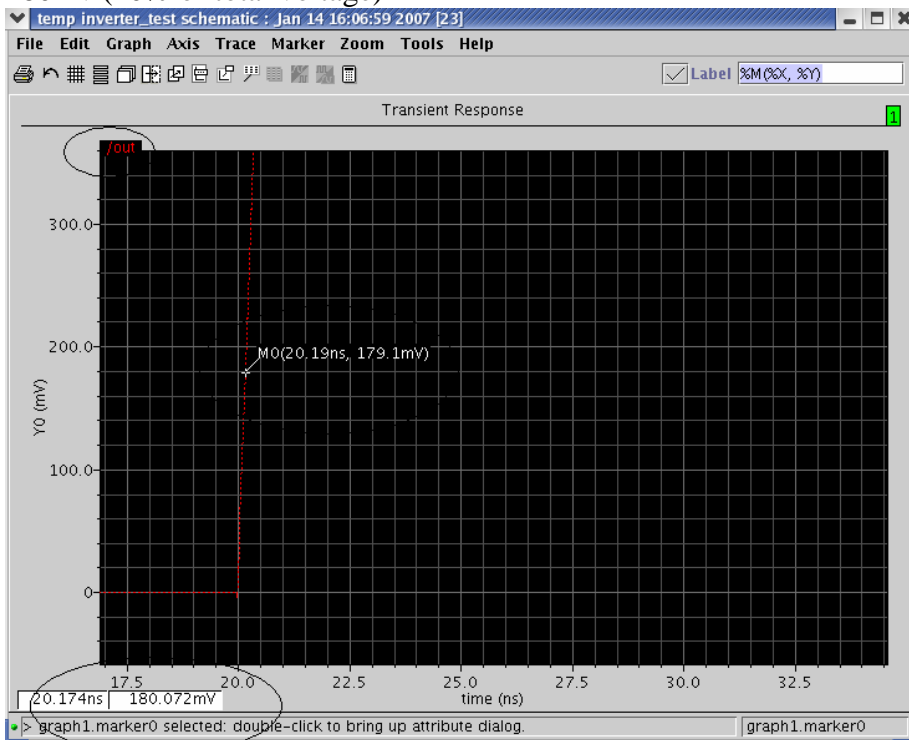


If you use “Outputs -> To Be Plotted ->Select from Schematic”, after successful simulation, the required signals are automatically plotted. Otherwise, you need to select nodes to plot after simulation by using “Results->Direct Plot->transient signal” and click the left mouse on the node (wire) voltage to be plotted and then ESC. The figure below illustrates the results of a transient simulation on an inverter. The icon pointed on the left side allows you to separate the waves.

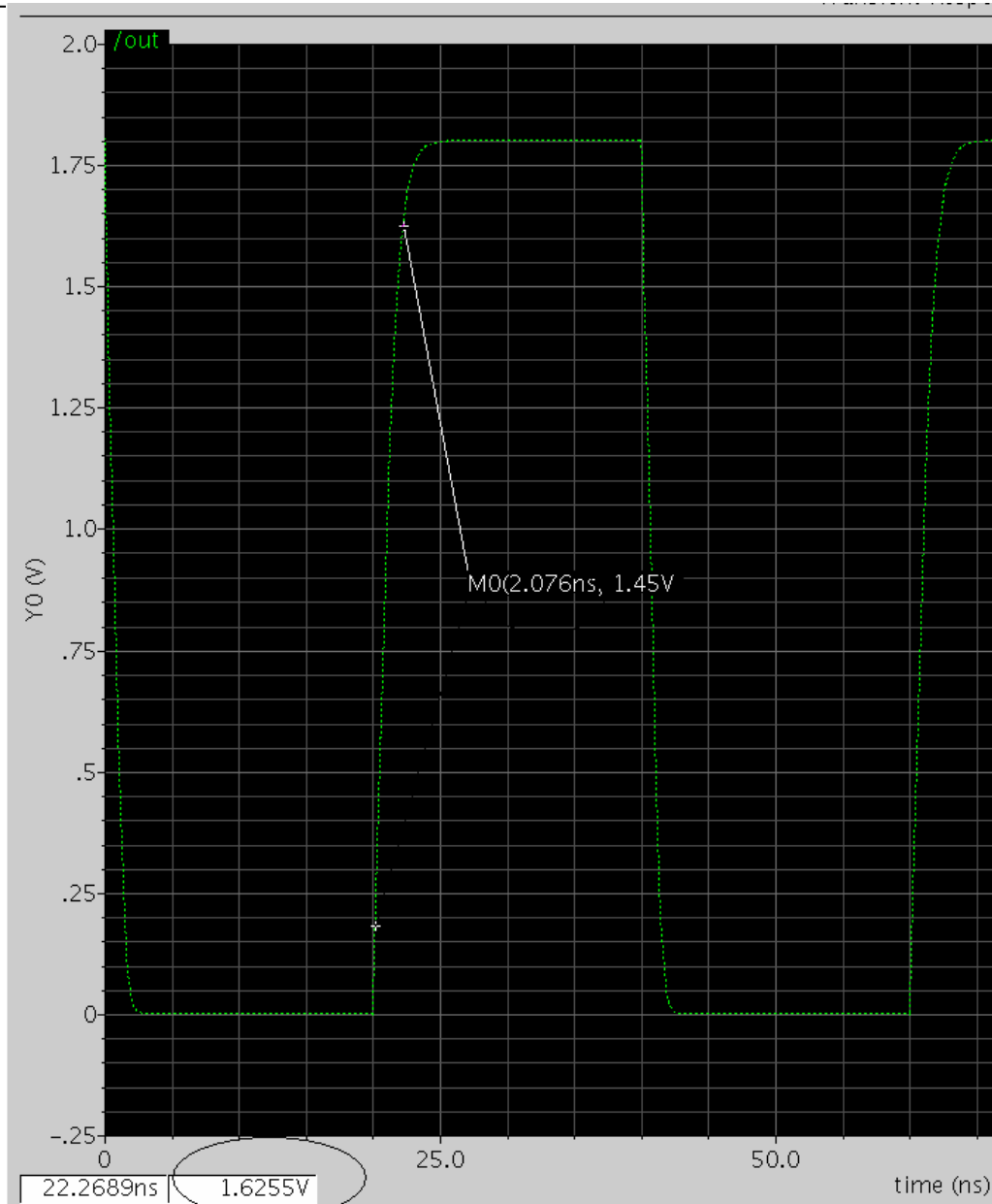
The figure below illustrates the results of a transient simulation on an inverter. The icon pointed on the left side allows you to separate the waves.



For example if you want to measure Trise of **out** signal press **m** button and put the pointer on 180mv (10% of total voltage)



The next stage is to push **a** and bring the pointer to 90% of the voltage (1.62v)
As you see Trise is =2.0764ns

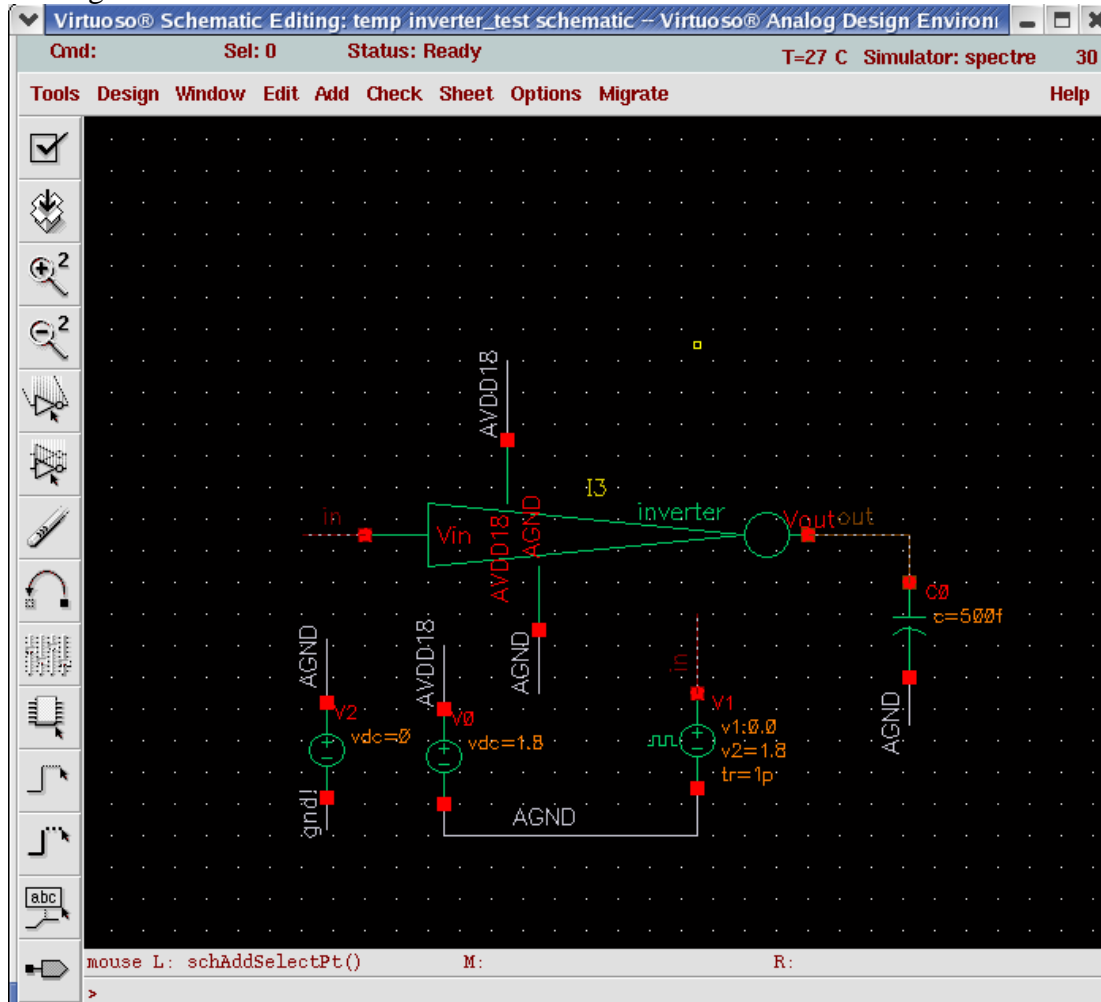


Before you exit click on session ->save state , so the the next time you'll enter analog environment instead of defining your simulation again . you will click session ->load state .

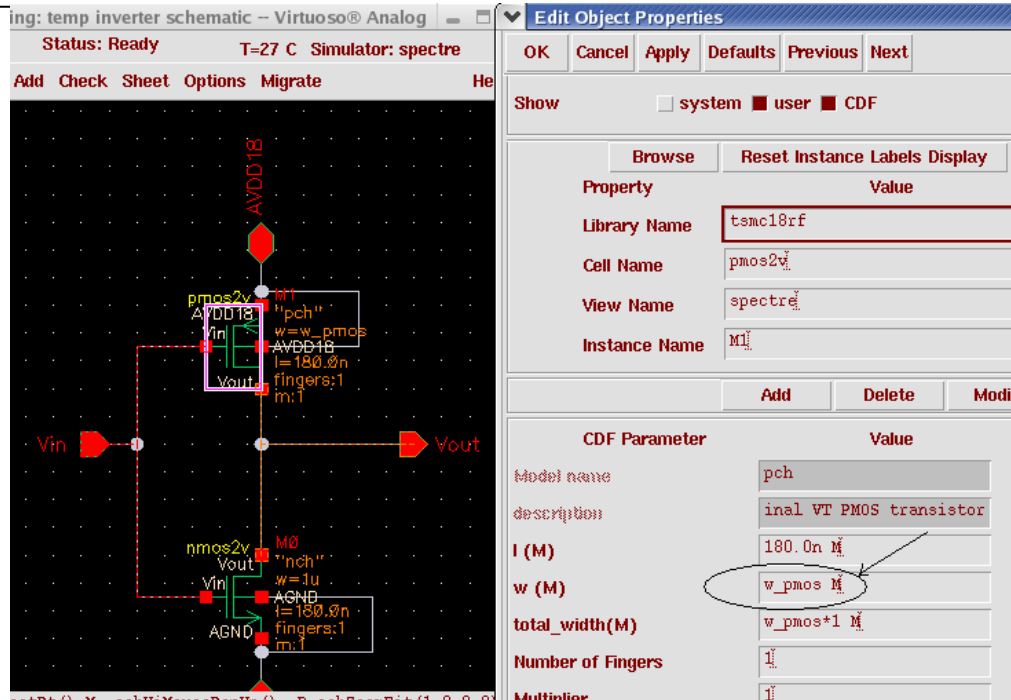
Parametric sweep

If you would like to compare some simulation by changing manually the value of voltage source, width or length of transistor, capacitance or any other parameter on your scheme you can do it automatically and save yourself a lot of time.

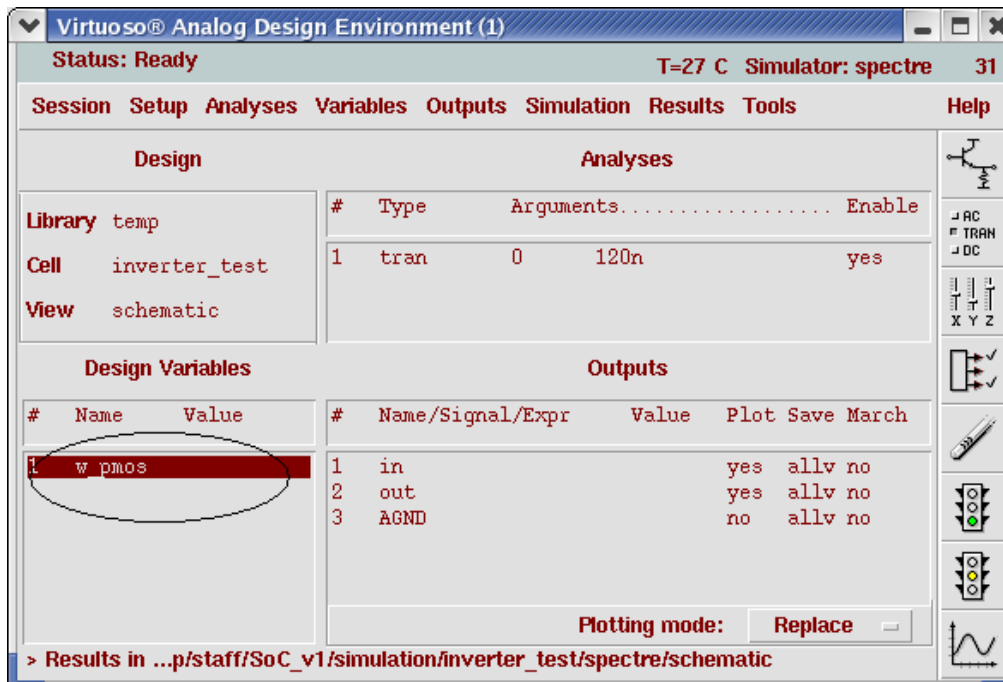
Now let's go back to our simulation:



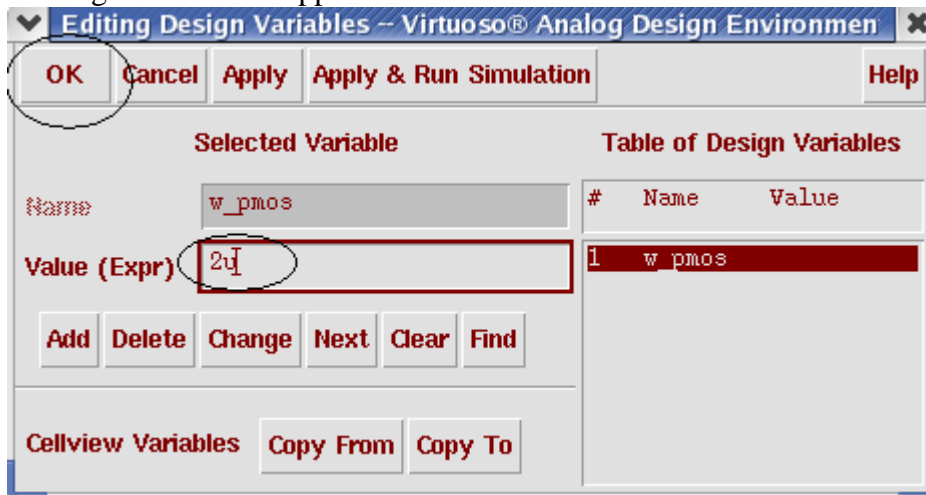
By pressing **shift x** (down in hierarchy) on the not symbol, you will enter the lowest hierarchy on the inverter. Next you'll press **q** while pointing on pmos and change the property.



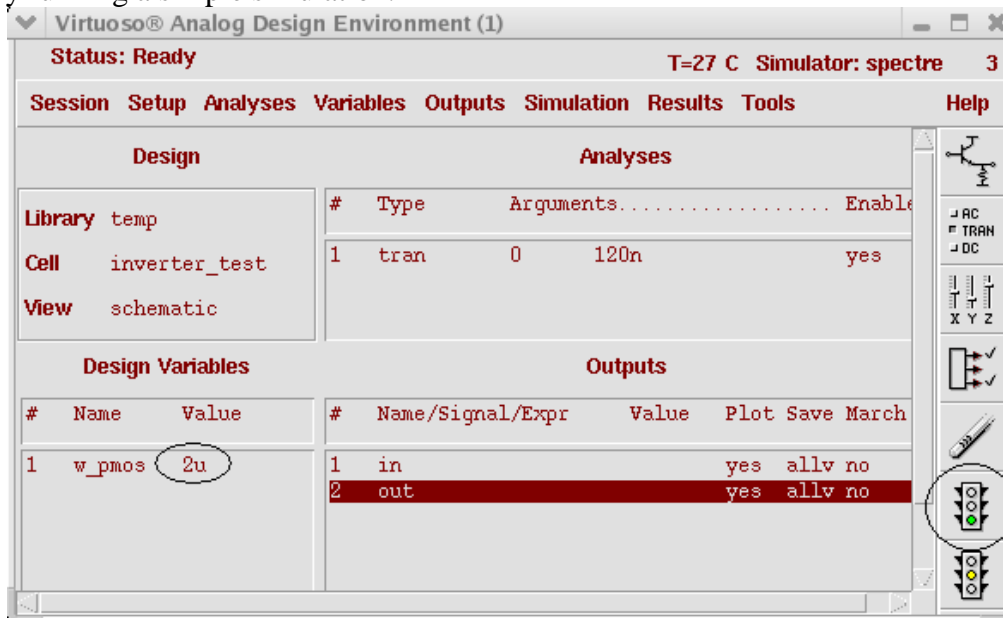
In the Analog Environment press **Variables->Copy From Cellview**
And the following will appear:



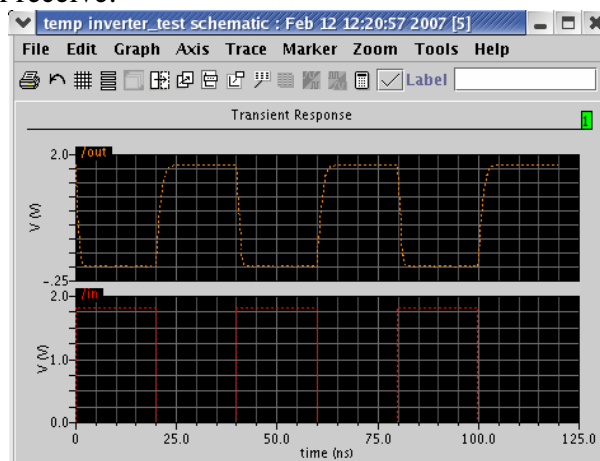
Very important: **don't** forget to define the default value of Design Variable by pressing twice on it the following window will appear:



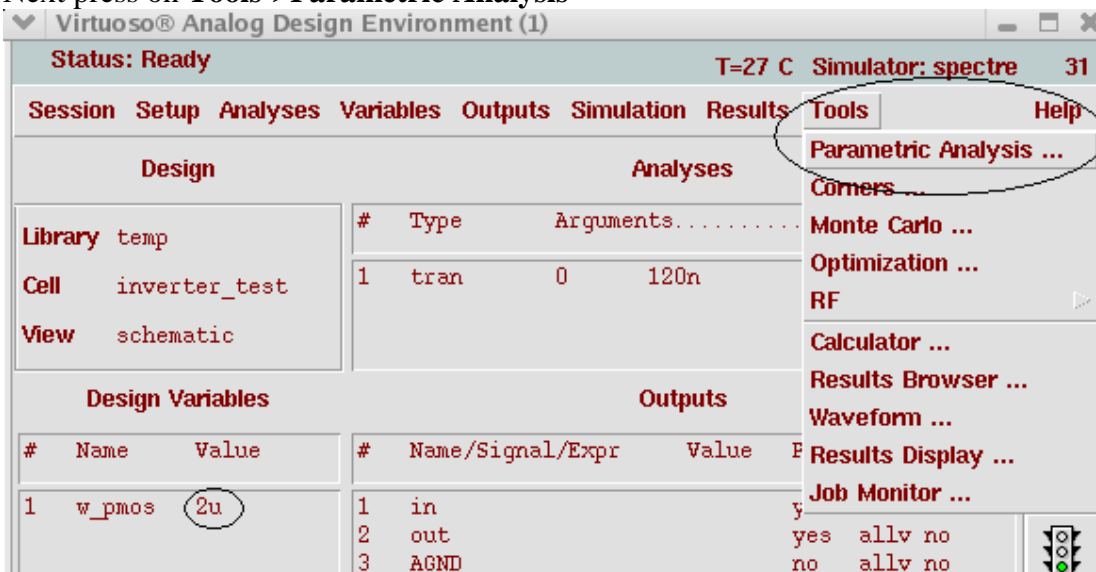
Write the value in Value(Expr) section and press **Ok**.
Before you will run Parametric Analysis **check** that the design variable default value is in range by running a simple simulation.



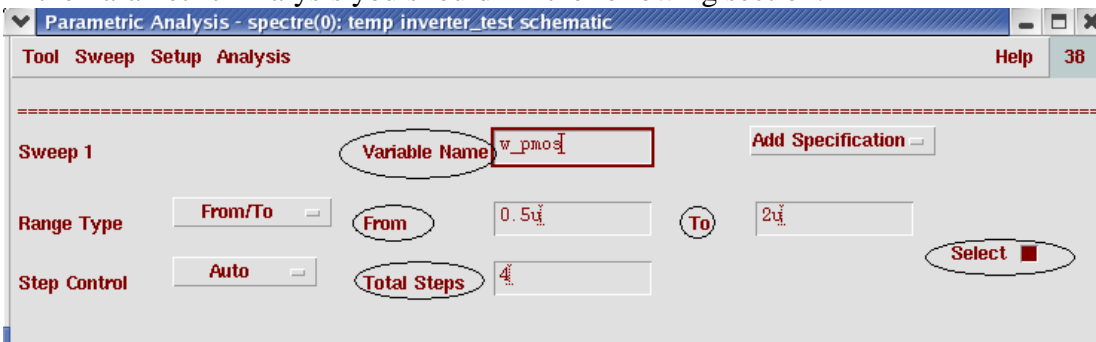
The waveform you will receive:



Next press on **Tools->Parametric Analysis**



In the Parametric Analysis you should fill the following section:



Variable Name: The parameter you want to change →w_pmos

From : first value

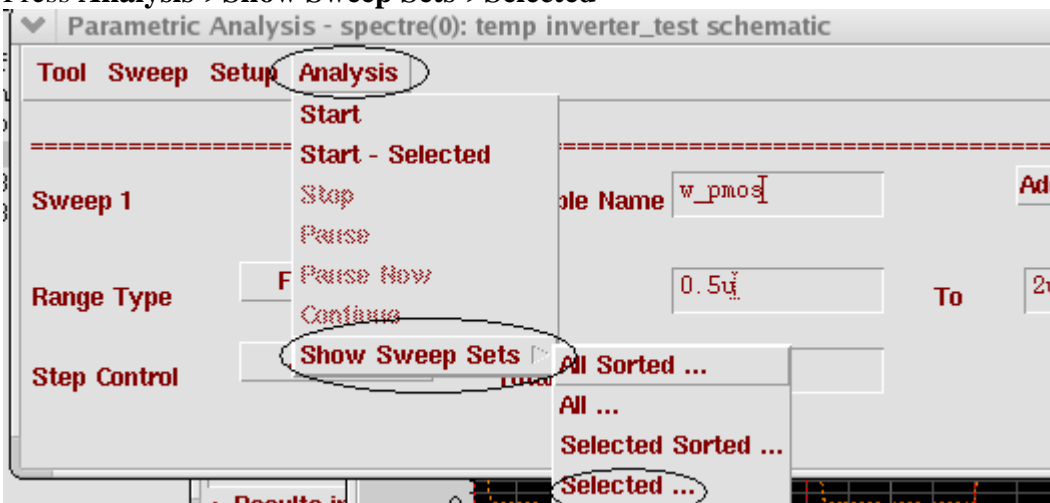
To: last value

Total Steps: exactly as it sounds

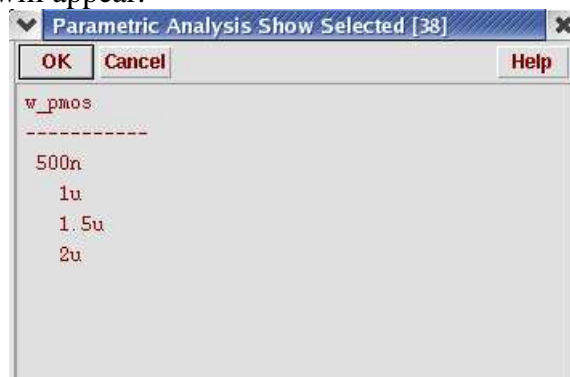
Also you have to press the **Select**

To be sure all the values you to be simulated will be simulated

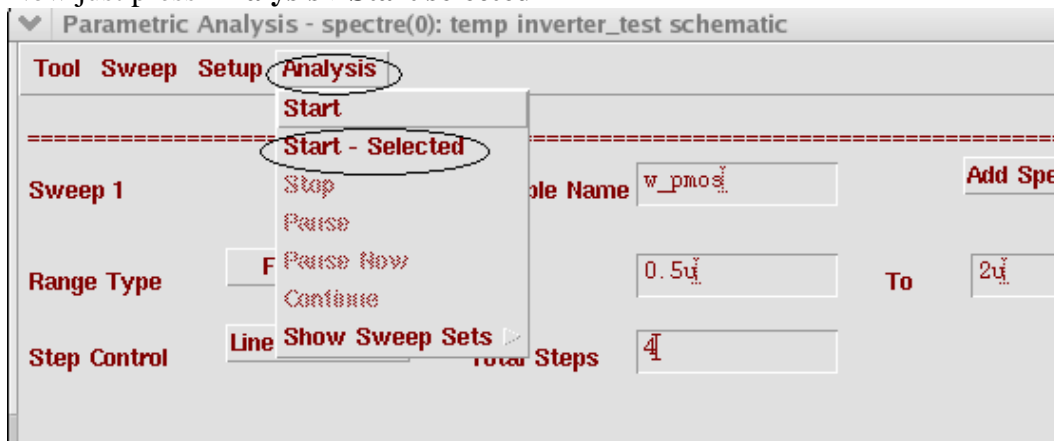
Press **Analysis->Show Sweep Sets->Selected**



The following window will appear:

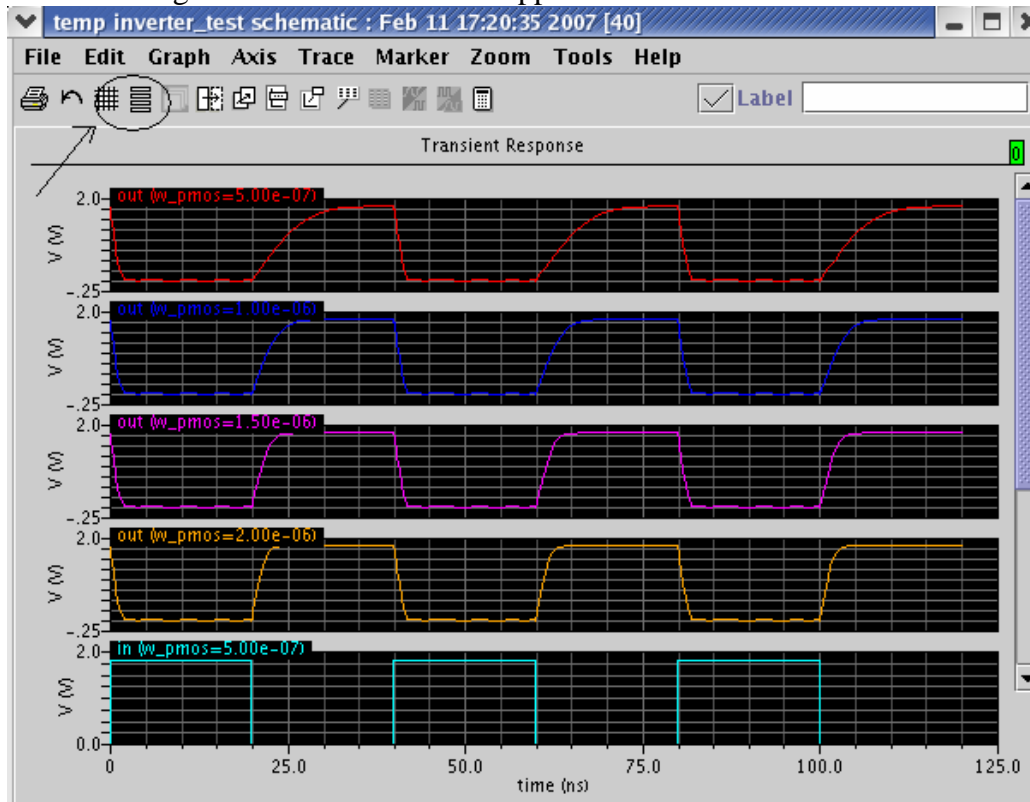


Now just press **Analysis->Start selected**



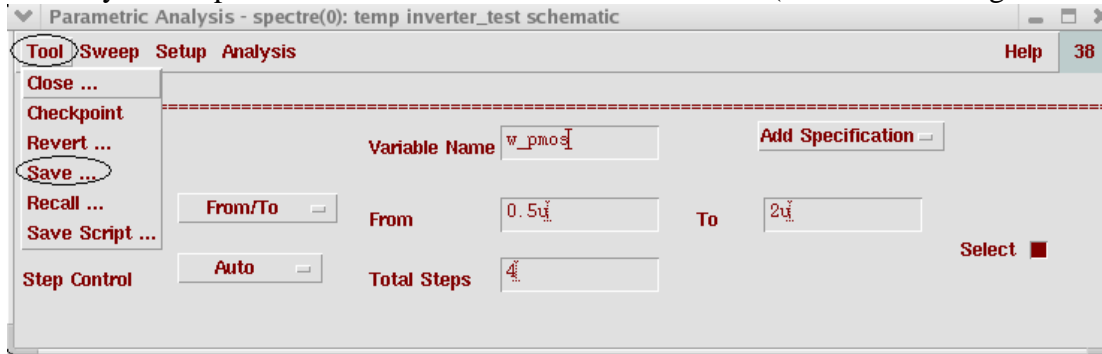
And the simulation will start !!!

The following waveform window will appear:

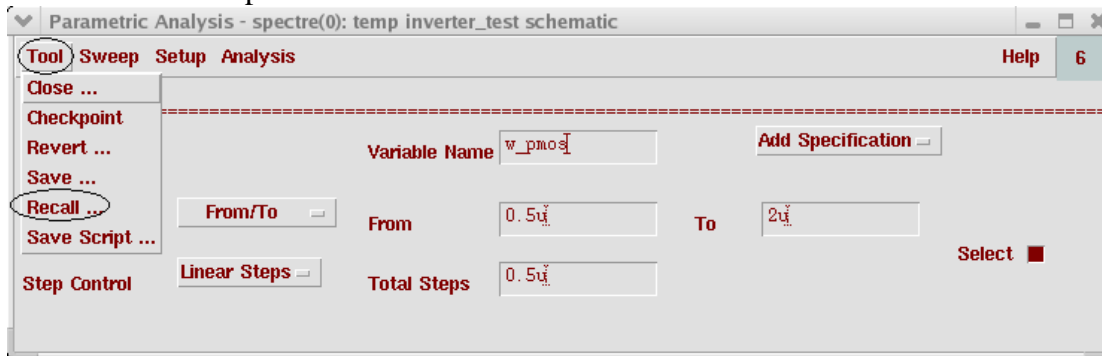


Press **Strip Chart Mode** button (pointed on the screen) to split the waves. As you can see there four different outputs for four different values of **w_pmos**.

Before you exit press **Tool->Save** in order to save the state (similar to Analog environment)



If you would like to load the current state in the future all you'll have to do is press **Tool->Recall** and press OK.



Shortcut for Cadence

General mouse commands

left-mouse → select/click
middle-mouse → over object brings up typical properties
right-mouse → repeat last operation

LAYOUT VIEW

I → create instance
q → property
f → full view
u → undo
C → copy
p → create wire path
shift x → down in hierarchy (new windows)
x → down in hierarchy (same window)
shift b → up in hierarchy
b → up to selected hierarchy
Ctrl z → zoom in
Shift z → zoom out
Ctrl p → create pin
o → create via
r → create rectangle
k → create ruler
Shift k → Remove all rulers
l → create label
Shift f → Display all hierarchy levels
Cntrl f → Display only top level hierarchy
Shift S → Search Instance
Shift C → Cut selected
z → zoom to box using left-mouse clicks
arrow → keys move around window
F3 → Command options
F4 → change wire editing mode - partial /full

SCHEMATIC VIEW

Right click on mouse and circuit the area ->zoom in on area

I → create instance
Q → property
F → full view
U → undo
U → redo
C → copy
W → create narrow wire
W → create Wide wire
R → rotate
l → label wire
shift e → down in hierarchy (edit mode)
e → down in hierarchy (read only mode)
Ctrl e → up in hierarchy
[] → zoom out / in
